Ray Stata of Analog Devices Speaks Out on

What's Wrong with Op-Amp Specs

Few products have more specs per cubic inch than operational amplifiers. It's no wonder that this is an immensely fertile field for Murphy's Law to raise havoc. Considering the number of variables to be juggled, and the relative inexperience of many op-amp users, it's not surprising that the circuits don't always play the first time around.

When manufacturers add the smoke screen of foggy specs, either deliberately or inadvertently (and I guess we are all guilty of this at one time or another), the poor user is really in trouble.

There's a bewildering array of numbers and most are just approximations.

Op amps are darned complicated. There are really lots of specifications, and most are only approximations of what's happening in the black box. Most parameters like voltage drift, current drift and open-loop gain are nonlinear functions of temperature; others, like common-mode rejection and common-mode impedance, are nonlinear functions of input voltage. And almost all parameters depend on supply voltages. Therefore, when you use a single number to specify a parameter, you must qualify the conditions of the measurements. Comprehensive graphs would be necessary to define performance completely.

Confronted with 50 more-or-less mysterious numbers, most engineers tend to select an op amp in terms of familiar values and to forget about the rest. An engineer who wants to replace a sensitive relay with a low-cost amplifier might simply concern himself with the output-current rating and neglect such factors as drift or gain.

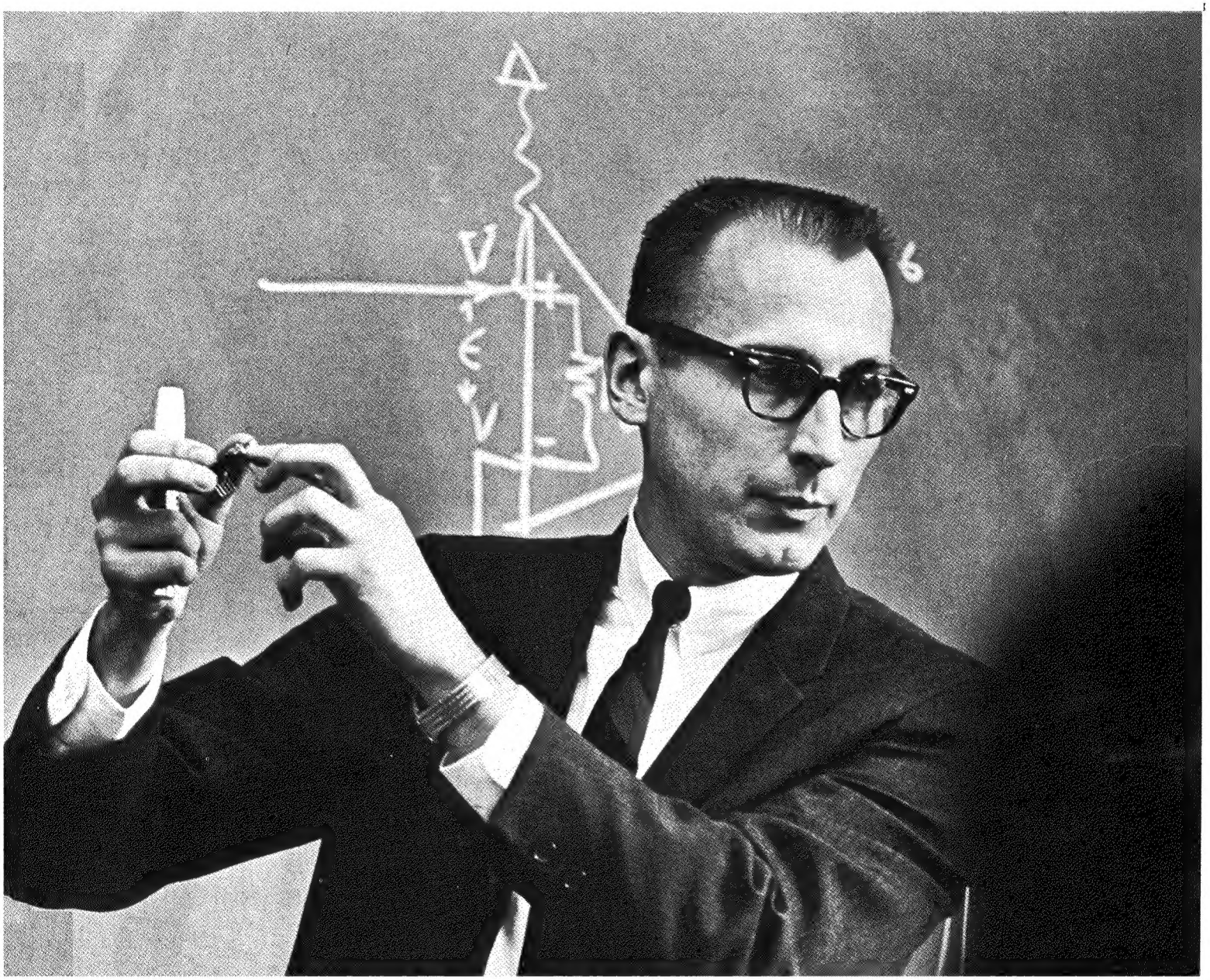
And there are no standards.

Then there's the lack of standards for op-amp specs. Though various efforts have been made to unify terms throughout industry, this has not yet been done, so manufacturers have loopholes for specsmanship.

Along with real, honest-to-goodness specsmanship, we find the inadvertent errors of omission. The holes in the spec, or usually, the lack of additional information, is not revealed until the engineer has assembled umpteen amplifiers into his product and the whole batch is waiting to be shipped. Very sad.

We were attending our first IEEE Show when a group of indignant engineers advanced on us and used us as whipping boys for the whole op-amp industry. They accused us of being con men. This we take in our stride when it's leveled at the competition, but these guys included us in their blast.

They had purchased a diff amp with a 5 μV/°C drift spec. The data sheet said that this number meant maximum voltage drift. What the sheet neglected to say was that the specs held only for steady-state temperature conditions. What happened during thermal transients was another kettle of fish that no numbers covered.



Though we were able to show that this point had been covered in an early application note, we certainly hadn't referred to it in spec sheets for any amplifiers. Actually we didn't know how to specify this mode of operation quantitatively. And some competitors had omitted the point.

Now, let's take a closer look at some of the major specifications and see how these problems come up.

There's more to voltage drift than meets the eye.

It can help to go back to first principles. We all know that a transistor's base-emitter voltage varies at roughly 2400 microvolts for every degree C change. This variation develops an output, or offset, exactly as if a true input of equal magnitude were driving the transistor. The use of differential pairs enables the net voltage offset to be drastically reduced because both transistors

can be matched so their offsets track within a few microvolts over the temperature range. This is how the amplifier comes to have a drift spec of 5 μV/°C instead of 2400 μV/°C; the transistors track within 5 μV for every 2400 μV of base-emitter drift, that is, for every 1°C rise.

But there's a flaw here. What happens if the base-emitter junctions are not at the same temperature? The spec states a figure for maximum drift, but this is really a tracking spec for base-emitter junctions at the same temperature.

Obviously, thermal gradients caused by adjacent heat-dissipating components can make nonsense of such specifications by making one junction hotter than the other. It only takes 0.1°C differential between the two junctions to develop 2400/10 = 240 microvolts offset. To say the least, this is a substantial offset for an op amp with a 5 μV/°C max drift spec.

In fact, offsets are caused not only by such obvious temperature-gradient sources as adjacent heat-dissipating elements and room-air drafts, but also by changes in the amplifier's own load current. Altering the output current from 2 mA to 20 mA produces an internal temperature transient that develops an offset due to unequal heating of the input transistor pair until temperature equilibrium is re-established. And when the amplifier has settled to its new output level, the input signal will invariably set the load current back to 2 mA, starting the problem all over again.

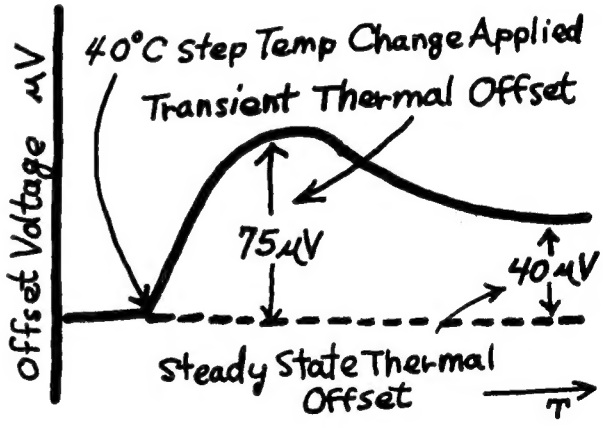
Offsets due to warmup and changes in operating conditions can be particularly annoying when an instrument or system is being adjusted. It takes only finger heat on one side of a differential amplifier to produce a distinctly-measurable offset error. How does one put performance specifications on such nebulous factors?

One way to sidestep the temperature-gradient error is to avoid the differential amplifier. A chopper-stabilized amplifier corrects automatically for transient offsets of this kind. Its error-sensing circuit is independent of mismatches between the transistors. But sometimes the chopper unit won't win. Apart from being twice as big and costly as a differential amplifier, the chopper-stabilized unit has only a single input terminal. (The other terminal is "used up" in the stabilizing circuit.) A single-ended amplifier can't easily be used in noninverting or differential circuits. So what you gain on the roundabouts breaks the rope on the swings.

Fortunately, some diff amps are inherently less susceptible to temperature gradients. Single-chip, dual-transistor front-end circuits cut down thermal inertia and reduce physical spacing between base-emitter junctions of each differential pair. Monolithic IC op amps are generally good on this score because of the small spacing between junctions.

Consequently, temperature transients never pull the two junctions more than a few hundredths of a degree apart. Such amplifiers offer a meaningful steady-state maximum voltage drift of about 1 μ/V°C, with a short-lived and worst-case offset of about 75 microvolts for 40°C thermal shock.

While an amplifier with a dual input transistor exhibits a considerable improvement in offset stability, there is no way to discern this fact in comparing the usual published offset-drift specifications. A user can get some idea of comparative thermal-gradient performance by making thermal shock tests, like dropping the amplifier in an oil bath 40°C above ambient. He'll get a response like this.



Okay, so we've raised one straw man and then beaten it down. But aren't there other problems that only specsmanship has solved thus far?

Zeroing can hide some second-order pitfalls.

What happens when you adjust an amplifier's offset potentiometer to zero its output at the selected working temperature? Not surprisingly, there's more to the process than meets the eye. And it's not always easy to tie up the sources of error in neat, crisp numbers.

The offset pot is frequently a variable resistor in series with a collector load resistor. The amplifier's output is zeroed by altering collector

current to change voltage balance between the two front-end transistors.

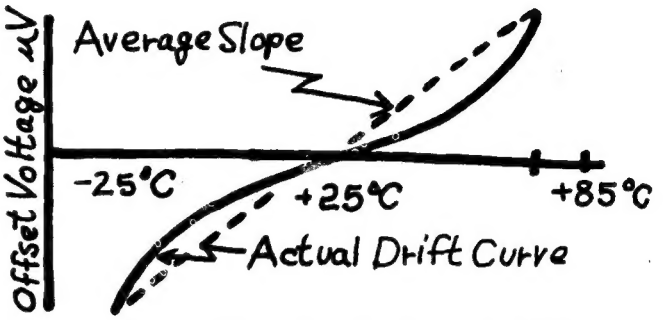
So What? Well, it turns out that there's a second-order effect that causes interaction between the actual value of collector current and the rate at which the transistor's base-emitter voltage drifts with temperature. Adjust collector current in one transistor of a matched differential pair and it no longer tracks the other as temperature varies. True, the adjustment modifies the base-emitter drift by only 0.7 μV/°C for each 250 μV change in emitter-base voltage or initial offset voltage.

But such differences can swamp the carefully-designed tracking specs of today's state-of-the-art differential amplifiers. For example, some chopperless differential amplifiers have better than 1 μV/C° maximum voltage drift. To zero an initial offset voltage of 1 mV with the internal balance pot in one of these amplifiers would introduce a change in temperature drift of 2.8 μV/°C. And that really screws up the works.

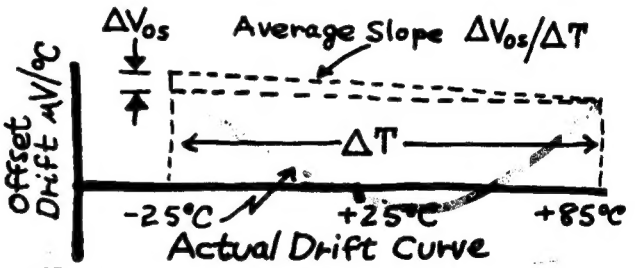
Some manufacturers neglect to point out the second-order effects caused by trimmer adjustments, but as op amp specs improve these effects can no longer be ignored. One must really know the condition of the balance resistor to specify voltage drift uniquely. We get around this by eliminating provisions for an internal offset trim on low-drift amplifiers and by recommending external offset biasing circuits.

Average drift is a trap. Remember the man who drowned while wading through a stream with an average depth of only four feet?

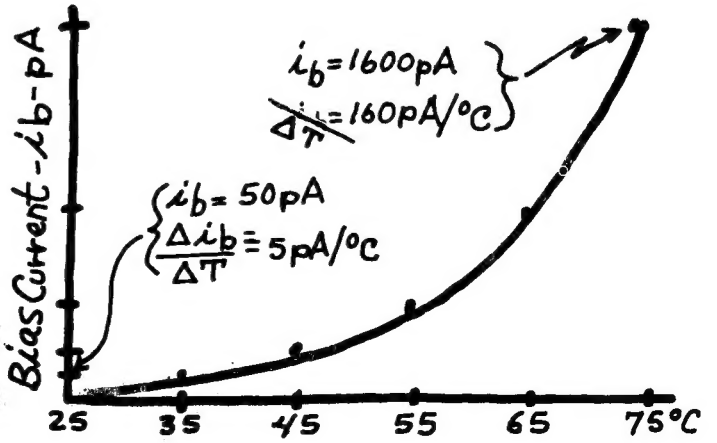
Neither voltage drift nor current drift are linear functions of ambient temperature. Accordingly, the numbers published for voltage drift and bias-current drift can refer only to average values, or to values at specific operating conditions. For example, an amplifier's total change in voltage offset for a temperature excursion from −25 to +85°C might be 2200 microvolts (referred to the input). The average drift rate over this interval works out to 2200/110° or 20 μV/C°. But when you look at the actual drift curve you see that the drift rate at the extremes of temperature can exceed the specified average drift rate by a substantial amount.



You have a special problem when the drift curve changes slope—a real live possibility. Here the average slope calculated by subtracting end points is entirely meaningless. Nonetheless, some manufacturers have taken advantage of this golden opportunity for specsmanship.



Perhaps trickier to interpret than the voltage-drift figures are the nonlinear errors caused by exponential variation of bias currents in FET and varactor-bridge amplifiers. Usually, the bias current at a given temperature is specified, and the spec reader is reminded that the bias current doubles for approximately 10°C temperature rise as it does here.



If a value of bias-current drift is given, it is usually quoted at room temperature, where the slope of the bias current versus temperature curve (i.e., drift) is shallowest. But at 85°C, the bias current and drift slope will be 64 times worse than at room temperature, making the FET amplifier a worse choice for high-temperature applications than some bipolar transistor types. This is not really a question of specsmanship, but it certainly requires that the user know his way around a spec sheet.

How much output do you really get?

An amplifier output rating of ±10 volts, ±20 milliamps implies that the user can drive a 500-ohm load at the full signal swing of 10 volts, 20 milliamps. For discrete-component op amps this is usually what such specs mean. But, integrated circuit manufacturers seem to have different ideas. "Sure you can get 10 volts output; certainly it will develop 20 milliamps," they say, but they often forget to add, "so long as you don't ask for them simultaneously." In fact, it is not unusual for an IC amplifier labeled as having a ±10 V, ±5 mA output to have a maximum power rating of only a fraction of the product of the VI figures given.

If an engineer needs an op amp with a relatively high output, he generally wants to know what gain he's getting at that current level. If 20 mA is the amplifier's full-load rating, it would be nice and simple if the manufacturer stated the amplifier's open-loop dc gain at this full load. Not all manufacturers do.

The op-amp user should know his amplifier's roll-off curve in order to build a circuit with adequate gain stability over the working frequency range. The manufacturer may be perfectly justfied in departing from the conventional 6 dB/octave frequency compensation to achieve desirable features like fast settling time, high slew rate, fast overload recovery, or increased gain stability over a wide range of frequencies.

But to obtain these improved features generally requires fast roll-off characteristics and therefore a propensity toward oscillation. Key to preventing instability, of course, is knowing that you have this kind of amplifier. You can then use one or more well known circuit techniques to tame the oscillations.

The great crime occurs when manufacturers use fast roll-off compensation to obtain improved published specs without giving an open-loop response curve or some other indication of what's going on.

Let's look at common mode, the specs we'd all like to forget.

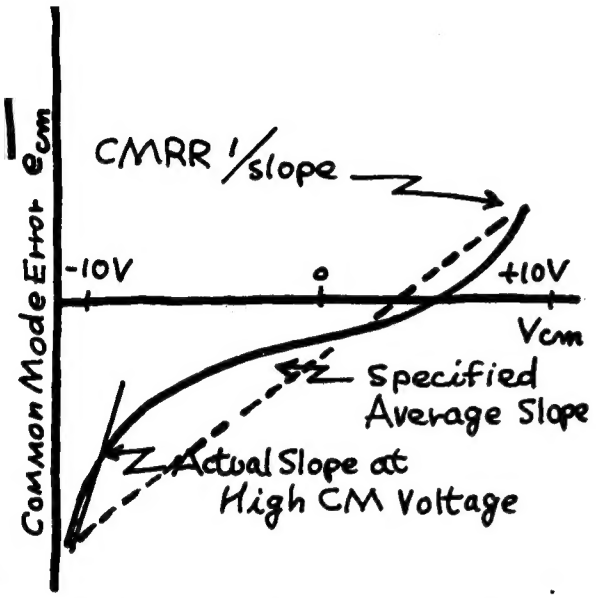
To many users the common-mode rejection ratio of an amplifier is a rather mysterious number that they'd like to forget. Many op-amp manufacturers feel the same way. In fact, if a particular amplifier has a poor common-mode spec, some manufacturers thoughtfully omit it from the data sheet.

Low-cost FET amplifiers are the worst culprits, with typical common-mode rejection ratios around 1000. This is exactly the kind of number that manufacturers would like to lose. They often do. For a noninverting amplifier circuit, the common-mode error is 1/CMRR, which works out to 0.1% for an amplifier with CMRR of 1000, or 60 dB. Recently, new circuit tricks have enabled manufacturers to overcome this fundamental limitation of low CMRR, but a FET amplifier with 100,000 CMRR tends to cost more than $100.

Picking a typical CMRR spec from measured op-amp data is great sport. The numbers vary over an enormous range — from 500:1 to as high as 100,000 for FETs — all seemingly at random. A reasonable way for a manufacturer to select a typical common-mode figure for his data sheet is to pick a value that is met by 70 or 80% of all units of that particular type. Some manufacturers, with considerable ingenuity, average all the test numbers to find a "typical" value. Tweaking up a few samples to get 100,000 CMRR can do great things for averages of this kind and can, of course, lead to very respectable-looking common-mode rejection figures.

As with drift, an amplifier's common-mode-rejection performance can vary with operating conditions, notably with the value of common-mode input voltage as we can see in the sketch. This leaves room for some really fancy footwork. For example, some well known FET types boast a common-mode voltage range of ±10 volts. But the common-mode rejection figures are specified for a ±5-V common-mode

range. It's possible for the CMRR to degrade by as much as a factor of ten when the applied common-mode voltage is raised from 5 to 10 volts.



Another difficulty with CMRR is that, since it's a nonlinear function of input common-mode voltage, a single spec number can at best give an average value over the test-voltage range. For small input-signal variation about some large common-mode voltage, the specified "average" CMRR gives little indication of the actual errors you can expect due to the steeper error slope at high voltages.

How full is the full-power response?

We all know that an amplifier rated at, say, 10-MHz unity-gain bandwidth, doesn't give full output-voltage swing at this frequency. Invariably, distortion caused by internal slew-rate limiting induces the manufacturer to specify the maximum full power frequency several decades lower.

Generally, an amplifier with 10-MHz unity-gain bandwidth would have a full-power response of about 1 MHz or maybe as low as 100 kHz. At the "small signal" unity-gain bandwidth, the achievable output-voltage swing is usually related to the swing at the full-power bandwidth by the ratio of the full-power response, f_p, to the unity-gain bandwidth, f_t. Thus, for example, you get only a 100-mV swing from a 10-V amplifier at unity-gain bandwidth for an amplifier with an f_p of 100 kHz and an f_t of 10 MHz.

One large problem with full-power-response specs is that no one really says what he means by the published minimum number. For one thing full-power response has nothing to do with amplitude vs frequency as the term "response" normally implies. Instead it is a measure of output distortion caused by slew-rate limiting.

But there can be monstrous difference depending on whether you set 1% or 10% as the acceptable distortion level. We have evaluated some amplifiers where the output looks a triangle at the specified full-power response. Where do you draw the line on the acceptable distortion level?

Distortion is only one consideration in setting the criteria for the full-power-response spec. A subtle, but very often more important side effect, is dc offset error due to rectification. Feedback signals developed by an unsymmetrical, distorted output, will not counterbalance the input signal at the amplifier's summing junction. So, the error signal is rectified by the amplifier's input stage, generating an undesirable offset voltage.

But how can such application factors be reasonably prevented? Should each data sheet be turned into a thesis, or may the manufacturer assume that his customers are already aware of the difficulties awaiting them? There is no easy answer for either the manufacturer or the customer.

Slewing rate for the most part is just another way of looking at rate limiting of the amplifier's circuitry. The slewing-rate specification applies to transient response while full-power response applies to steady state or continuous response. For a step-function input, slewing rate tells how fast the output voltage can swing from one voltage level to another. Fast amplifiers will slew at up to 300 V/μs, while amplifiers designed primarily for dc applications often slew at 0.1 V/μs or less.

Maximum slew rate, S, is related to full-power response f_p by $S = 2\pi f_p E_o$. As the voltage swing is reduced below the peak output, E_o, the operating frequency can be proportionately increased beyond f_p without exceeding the slewing rate. For many amplifiers the slewing rate may differ in the inverting and noninverting configurations — a fact that is not always apparent from published specs. Moreover, there is almost always a difference in slewing rate between fall time and rise time, and between positive and negative output signals. Opportunities for specs-

Who is Ray Stata?

A soft-spoken man with a wry sense of humor, Ray Stata doesn't publicly expose the fact that he's a dynamo. He has packed more experience in his 33 years than many men twice his age. He earned his BS and MS in EE at MIT, then worked at MIT's Instrumentation Lab before he went for some industrial experience at HP.

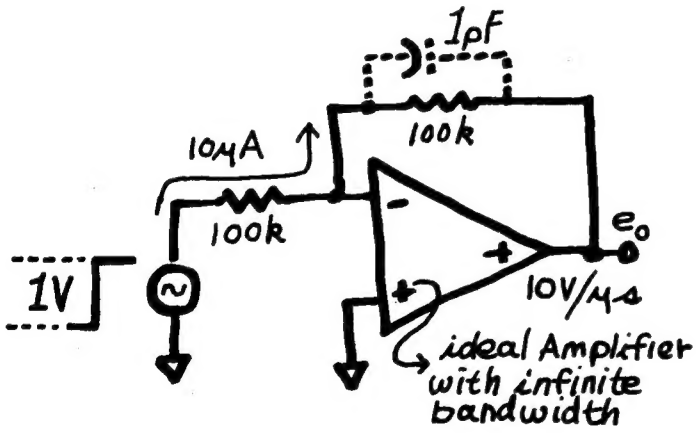
In 1961, just three years after he obtained his MS, he and Matt Lorber started Solid State Instruments on a shoestring. They sold that company and used the proceeds to start Analog Devices in January 1965. In just three years, they brought the sales level to a $5-million annual rate.

Ray enjoys writing on op-amp theory and applications as much as he enjoys building companies. A Boston Symphony enthusiast, he retains an active interest in music and in his record collection.

His greatest joy however (and the joy of his wife Maria) comes from his four-month-old son, Raymond Paul, who has not yet developed an interest in operational amplifiers, symphonic music or building companies.

manship arise here since many possible slopes can be measured.

A recurrent problem in our applications department is the irate telephone call from a customer claiming that our amplifier does not meet its slewing-rate spec. Closer inquiry typically shows that the customer is trying to obtain 100 V/μs slew rate with a circuit like this one.



The problem here is that the inevitable 1 pF of stray capacitance must be charged by the 10-μA signal current. This limits the output slew rate to 10 V/μs regardless of how fast the op amp may be. With an input impedance of 10 kΩ or less, the customer would obtain the desired 100 V/μs slewing rate. In other words, you cannot get fast response from an inverting amplifier when using high input impedance owing to the slugging effect of stray capacitance.

Settling time is a parameter of increasing interest. This spec defines the time required for the output to settle within a given percentage of final value in response to a step-function input. Common accuracies of interest are settling time to 0.1% and 0.01%. Heretofore, engineers have been forced to use slewing rate and unity-gain bandwidth as rough indicators of relative settling-time performance when comparing or choosing amplifiers, since no other data are given. As it turns out, these two specs have little bearing on settling time, particularly to 0.01%.

Manufacturers now realize this and are beginning to publish settling-time figures. The hooker here is that settling time is really a closed-loop parameter (while all other op-amp specs are open-loop parameters), and therefore depends on the closed-loop configuration and gain. Fortunately, even when published for only one gain, usually unity gain, it serves as a realistic yardstick for comparing amplifier performance.

The few examples I've shown illustrate the tremendous difficulties in specifying op-amp performance and the many pitfalls confronting the user. In the long run the user and manufacturer are on the same side in seeking unambiguous communications. One needed step is for an industry group to establish standards on definitions and test circuits. The use of op amps is growing very rapidly and this move is long overdue.

There's one further point that can be most important of all. An engineer should breadboard his critical circuits instead of relying totally on paper designs. Better yet, he should contact the applications department of an op-amp manufacturer to review his problems. Few engineers take advantage of this free service or give proper weight to this important aspect of picking a vendor. **EEE**

ANALOG DIALOGUE

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User's Guide to Applying and Measuring Operational Amplifier Specifications

By Ray Stata

Editor's Note;

This article is the result of many requests for a definitive article discussing the definitions and testing of op-amps. Keep on sending in your requests . . . we will try to fulfill them.

SINCE THERE ARE NO established standards for operational amplifier specifications we shall discuss here the terms used by Analog Devices to define operational amplifier characteristics as well as the limitations which must be observed in applying the published data to actual circuits. Wherever possible we show the test circuits used to measure these parameters. Although these test circuits are applicable to a wide range of operational amplifiers, special amplifiers such as FET, chopper stabilized or ultra fast response amplifiers may require changes in the recommended circuit values or in some cases different test methods to measure their specifications. As a general rule the power supply for these measurements should have line and load regulation of about 0.1% and ripple should be no more than a few millivolts.

Figure 1 gives a simplified equivalent circuit for an operational amplifier showing many of the sources of error which are discussed in the text The specifications should be referenced to this diagram to predict their effect in a closed loop circuit. For a single ended amplifier you would assume that the plus or non-inverting input is grounded.

OPEN LOOP GAIN

Open loop gain, A, is defined as the ratio of output voltage to error voltage e_ε between inputs as shown in figure 1. Gain is usually specified only at DC (A_o), but in many applications such as AC amplifiers the frequency dependence of gain is also important. For this reason the typical open loop gain response is published for each amplifier. The open loop gain response of most amplifiers can be approximated by figure 2.

ALSO IN THIS ISSUE

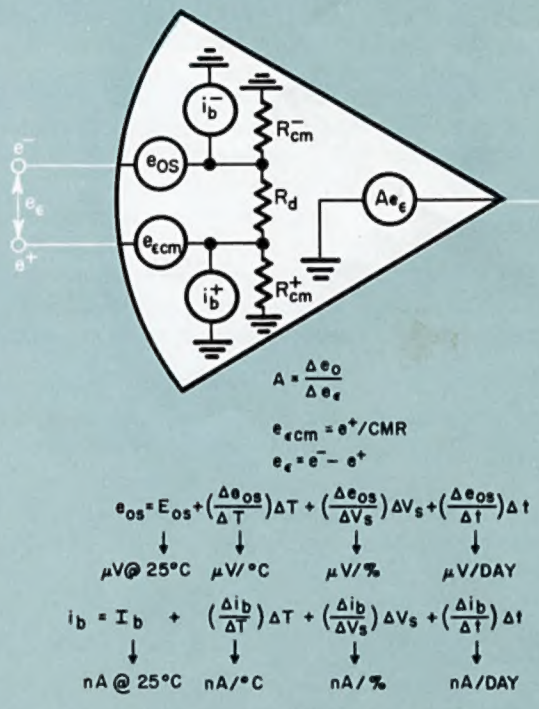


FIGURE 1. OPERATIONAL AMPLIFIER EQUIVALENT CIRCUIT

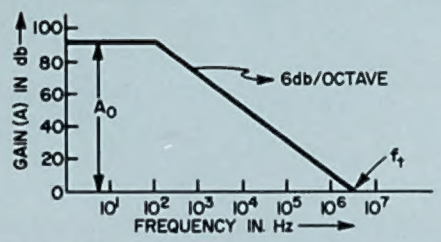


FIGURE 2. TYPICAL OPEN LOOP GAIN RESPONSE

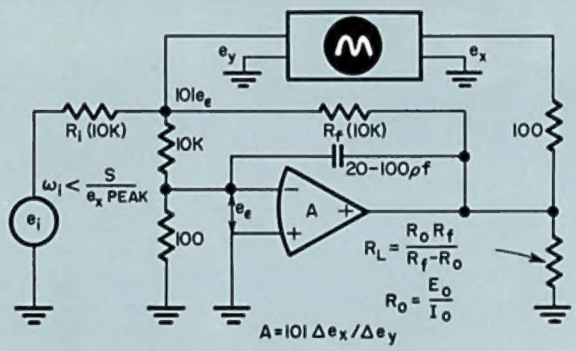


FIGURE 3. OPEN LOOP GAIN TEST CIRCUIT

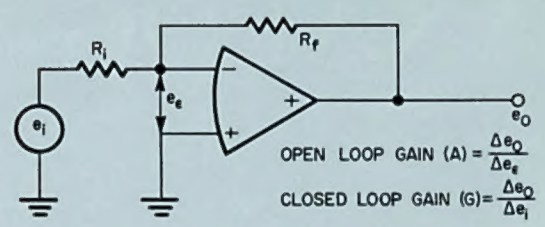


FIGURE 4. CLOSED LOOP CIRCUIT

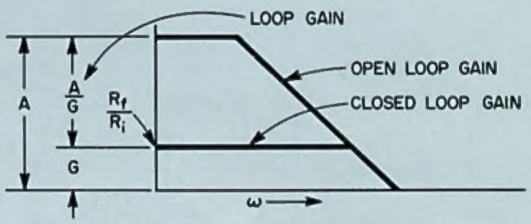


FIGURE 5. DETERMINATION OF LOOP GAIN

Open loop gain changes with load impedance (R_L), ambient temperature and supply voltage. As a rule, open loop gain will not change more than a factor of 10 between rated load and no load conditions. Most operational amplifiers have a positive gain temperature coefficient of about 0.5 to 1%/°C and gain changes with supply voltage at about 2%/%. Analog Devices specifies all open loop gains at rated load, 25°C and rated supply voltages.

A practical circuit for measuring open loop gain over a range of frequencies is shown in figure 3. The voltage divider on the negative input boosts the sensitivity of the error voltage by 100 times which makes it possible to measure gains up to one million. At low frequencies open loop gain is constant so that DC gain can be measured by a low frequency signal (about 5Hz). The voltage divider may not be necessary for low gain amplifiers (below 20,000) and it is not recommended for measuring gain at high frequencies where open loop gain is less.

At very best, noise pick up is a problem for measuring high gains and care must be taken to adequately shield the test circuit. At high frequencies the amplitude of the output voltage must be reduced to avoid exceeding the slewing rate of the amplifier. For this reason the output voltage should be adjusted, so that $e_x(\text{peak}) < \text{slew rate}/\omega_i$, where ω_i is the test frequency.

SIGNIFICANCE OF OPEN LOOP GAIN

Operational amplifiers are rarely used open loop. Instead negative feedback is used around the amplifier to improve the accuracy of the circuit. This introduces a second term, closed loop gain (G), which is defined as the gain of the circuit with feedback. The simple inverting amplifier in Figure 4 illustrates this point.

Linearity, gain stability, output impedance and gain accuracy are all improved by the amount of feedback. Figure 5 graphically illustrates the relation between open loop gain and closed loop gain.

The excess of open loop gain over closed loop gain is called loop gain. (Subtraction of dB is equivalent to arithmetic division.) The improvement of open loop performance due to feedback is directly proportional to loop gain. As a general rule for moderate accuracy, open loop gain should be 100 times greater than the closed loop gain at the frequency, or frequencies, of interest (that is loop gain = 100). For higher accuracy, loop gain should be 1000 or more. To illustrate, we recall that open loop gain stability for most operational amplifiers is about 1%/°C. With loop gain of 100, closed loop gain stability would be 100 times better or 0.01%/°C. Likewise, closed loop output impedance would be 100 times less than open loop output impedance with a loop gain of 100.

RATED OUTPUT VOLTAGE AND CURRENT

Rated output voltage, E_o, is the maximum peak output voltage which can be obtained at rated output current before clipping or excessive non-linearity occurs. This measurement is made at rated power supply voltage; at other supply voltages the output will swing to within about 4 volts of the supply voltage. Also the output voltage swing will increase somewhat at lower load current. Rated output current, I_o, is the minimum guaranteed value of current at the rated output voltage. Load impedance less than E_o/I_o can be used but E_o will decrease, distortion may increase and open loop gain will be reduced. Driving large capacitance loads at high frequencies will present a low load impedance which may then exceed the rated output current. Any convenient circuit such as figure 3 or figure 6 can be used to measure E_o and I_o.

UNITY GAIN SMALL SIGNAL RESPONSE

Unity gain small signal response, f_t, is the frequency at which the open loop gain becomes unity or zero dB (see figure 2). "Small signal" indicates that in general it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew rate limiting. Therefore in both measuring f_t and using the amplifier at high frequencies, the output voltage swing must be restricted to avoid slew rate limiting. This implies that the peak output voltage, e_o, for a sinusoidal signal at the unity gain frequency, f_t, must be less than $S/2\pi f_t$, where S is the slew rate.

For amplifiers with symmetrical response on each input, f_t may be measured by either the inverting circuit of figure 6 or the non-inverting circuit of the figure 7. Some units such as chopper stabilized amplifiers or wideband amplifiers with feed forward design have fast response only on the negative input which restricts testing and use to the inverting circuit. Remember that the closed loop unity gain response of figure 6 will be about one half the open loop unity gain response due to the loading of the feedback network. Moreover, large values of feedback resistance when coupled with stray capacitance may reduce the closed loop response and therefore the smallest possible value of R_f should be used, the limit being set by output current capability I_o.

Sometimes f_t is called unity gain-bandwidth product which implies that open loop gain at other frequencies can be predicted from this number. However, gain bandwidth product is constant only for amplifiers with 6dB/octave roll off! For fast roll off amplifiers, gain bandwidth product increases with gain and thus we publish the open loop response curve to give typical gain at each frequency.

FULL POWER RESPONSE

The large signal and small signal response characteristics of operational amplifiers differ substantially due to dynamic nonlinearities or transient saturation. An amplifier will not respond to large signal changes as fast as the small signal bandwidth characteristics would predict. The most prominent contributor to large signal response limitations is slew rate limiting in the output stages. Circuit and transistor capacitances can be charged and discharged only so fast due to the limited dynamic range of the driving circuits. Transient saturation can also occur in the input stages of the amplifier due to overloading the input stage or due to common mode voltage slew rate limiting, but this is rarely a problem as compared to saturation of the output stages.

Full power response, f_p, is the maximum frequency measured at unity closed loop gain, for which rated output voltage, $\pm E_o$, can be obtained for a sinusoidal signal at rated load without distortion due to slew rate limiting. Note that this specification does not relate to "response" in the sense of gain reduction with frequency. Instead it refers only to distortion in the output signal caused by slew rate limiting. For a sinusoidal signal, the maximum slope or rate of voltage change occurs at zero crossing and is proportional to the peak amplitude and the frequency. Thus we see that to a first approximation slew rate, S, and full power response, f_p, are related by equation 1.

$$\left.\frac{de_o}{dt}\right|_{max} = 2\pi f_p E_o = S \qquad \text{(equation 1)}$$

As the voltage swing is reduced below rated output, E_o, the operating frequency can be proportionally increased without exceeding the slew rate, S. In the limit the operating frequency approaches the unity gain bandwidth, f_t, and the corresponding voltage signal defines the maximum peak amplitude for "small signal" unity gain response. The circuits of figure 6 or figure 7 can be used to measure full power response depending on whether inverting or non-inverting parameters are measured. Where dynamic saturation of the output stages is the primary cause for slew rate limiting either test circuit will give equivalent results. For very fast response amplifiers, load capacitance and/or capacitance from the output to the negative input will cause apparent slew rate limiting and consequent degradation of full power response. This is due to saturation of amplifier output current in charging these capacitances and therefore such capacitances must be low.

Output distortion can be measured either by a distortion meter on the output or by observing a Lissajon pattern on an oscilloscope. There is no industry wide accepted value for the distortion level which determines the full power response limitation, but a number like 1% to 3% is a reasonable figure. One subtle point here is that closed loop output distortion depends on the amount of feedback or loop gain and therefore it depends on the closed loop gain of the measurement. Full power response is generally measured at unity gain where loop gain is the highest. At higher closed loop gains output distortion will increase for the same full power response frequency.

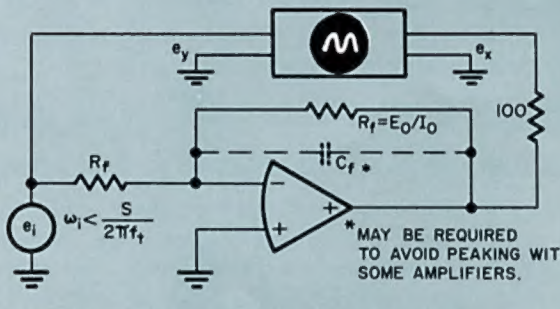


FIGURE 6. INVERTING CIRCUIT FOR MEASURING f_t, f_p, S, T

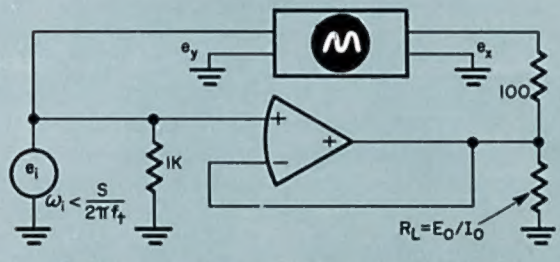


FIGURE 7. NONINVERTING CIRCUIT FOR MEASURING f_t, f_p, S, T, E_{cm}

In many applications the additional distortion which is caused by exceeding the full power response can be comfortably ignored. However, a far more serious effect, often overlooked, is that a DC offset voltage can be generated when the full power response is exceeded due to rectification of the unsymmetrical feedback waveform or due to overloading the input stage with large distortion signals at the summing junction.

These more subtle points in measuring full power response as well as the attendant side effects suggest the circuit of figure 8 as more satisfactory test circuit. By viewing the error voltage at the summing junction on an oscilloscope, distortion signals are more easily detected, signal generator distortion is eliminated from the measurement and frequency dependent DC offset can be readily observed.

SLEWING RATE

The origins of slewing rate limitations were discussed in the previous section. Slewing rate, S, usually expressed in volts/μsec defines the maximum rate of change of output voltage for a large step change.

Equation 1 suggests a convenient method to measure slewing rate by first measuring full power response, f_p, and then calculating S. Although this test method yields usable results for most amplifiers in most applications, the relationship of equation 1 does not apply under all conditions. First, slewing rate is a non-linear function of output voltage and equation 1 measures slewing rate only at zero volts output. This second order effect can usually be safely ignored in most applications. However, for certain amplifiers, particularly fast response types, the slew rate may be higher than that predictable from f_p. In these cases f_p is limited by factors other than slew rate such as DC offset errors which are generated by the rectification of large high frequency error voltages.

A more direct method to measure slewing rate is to apply low frequency square waves (about 100Hz) to the input of figure 6 or figure 7 which cause full voltage swing at the output and to observe the rise time from 10 to 90% on an oscilloscope (see figure 9). Small feedback resistors must be used to avoid degradation of slewing rate due to stray capacitance.

In applying operational amplifiers remember that repetitive input waveforms whose rise time exceeds the amplifier's slewing rate will generate voltage spikes at the summing junction. These spikes are usually unsymmetrical and are also usually clipped unsymmetrically by the input circuit of the amplifier — either or both of which effects will cause DC offsets at the output.

OVERLOAD RECOVERY

Overload recovery, τ, defines the time required for the output voltage to recover to the rated output voltage E_o from a saturated condition. For this test the circuit of figure 6 or 7 is used with an input square wave adjusted to be 50% greater than the voltage required to saturate the amplifier output. The square wave frequency should be adjusted to about 100Hz and the input-output signals should be compared on a dual trace oscilloscope as illustrated in figure 9.

In some amplifiers the overload recovery will increase for large impedances (greater than 50KΩ) in the input circuit, either the summing impedance for figure 6 or the source input for figure 7. Published specifications apply for low impedances and assume that overload recovery is not degraded by stray capacitance in the feedback network.

Normally, overloaded recovery time runs about one millisecond. For the inverting configuration an external clamp circuit can be added to improve overload recovery as illustrated in figure 10. This circuit prevents the output from saturating and therefore circumvents any delays due to overload recovery. The only constraint for proper operation is that input current (e_i/R_i) shall be approximately less than the rated output current I_o minus the load current. The clamp circuit cannot be used with the non-inverting and differential configurations.

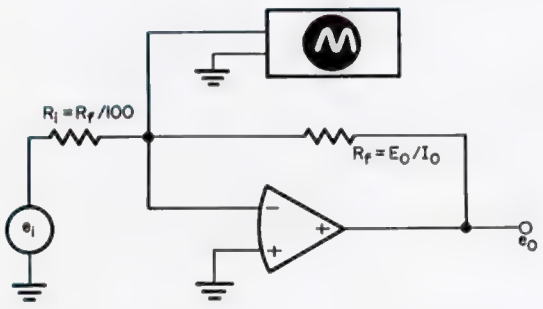


FIGURE 8. MEASURING FULL POWER RESPONSE

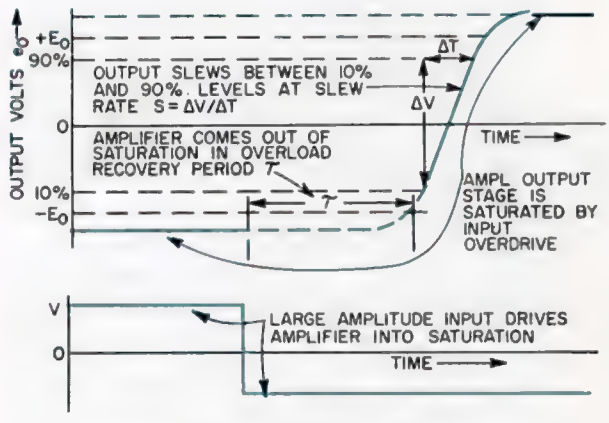


FIGURE 9. OVERLOAD RECOVERY AND SLEW RATE ILLUSTRATION

INITIAL OFFSET VOLTAGE

Offset voltage, e_{os}, is defined as the voltage required at the input from a zero source impedance to zero the output, at any temperature, supply voltage and time (see figure 1). Initial offset voltage, E_{os}, defines the offset voltage at 25°C and rated supply voltages. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer. Some amplifiers are internally trimmed to guarantee some maximum limit on initial offset (usually ±1mV) which means that in certain applications the external trim pot can be eliminated. On special order any amplifier from Analog Devices can be internally trimmed to ±1mV initial offset or less. Initial offset can be measured with the circuit of figure 11, where an appropriate fixed resistor is substituted for the external trim potentiometer. There is a warm up drift of offset voltage following the application of power supply voltage and it is recommended that you let the amplifier stabilize for at least 15 minutes before making measurements.

INITIAL BIAS CURRENT

Bias current, i_b, is defined as the current, at any temperature, supply voltage and time, required at either input from an infinite source impedance to zero the output assuming zero common mode voltage. For differential amplifiers bias current is designated by i_b^- for the negative input and by i_b^+ for the positive input. For single ended amplifiers, like chopper stabilized units, bias current refers to the current at the negative input only.

Initial bias current, I_b, is the bias current at either input measured at 25°C, rated supply voltages and zero common mode voltage. The designation (0,+) or (0,−) indicates that no internal compensation is used to reduce initial bias current so that the polarity is always known. The sign tells to which power supply voltage an external compensating resistor should be connected to zero the initial bias current. The designation (±) indicates that internal compensation has been used to reduce initial bias current and that the residual bias current can be of either polarity. In general compensating initial bias current has little effect on the bias current temperature coefficient. The circuit of figure 11 is used to measure initial bias current.

INITIAL DIFFERENCE CURRENT

Difference current*, i_d, is defined as the difference between the bias currents at each input from an infinite source required to zero the output assuming zero common mode voltage. The input circuitry of differential amplifiers is generally symmetrical so that bias current at each tends to be equal and tends to track with changes in temperature and supply voltage. Usually difference current is 3 to 5 times less than bias current at either input, assuming that initial bias current is not compensated. If the impedance as seen from each input terminal to ground is balanced then offset and drift errors are proportional to difference current rather than to bias current. In most applications, if the external impedances at each input are balanced then there is no particular advantage in using an amplifier where initial bias current is internally compensated. Initial difference current, I_d, the difference current measured at 25°C and rated supply voltage, can be measured by the circuit of figure 11.

*Previously called offset current.

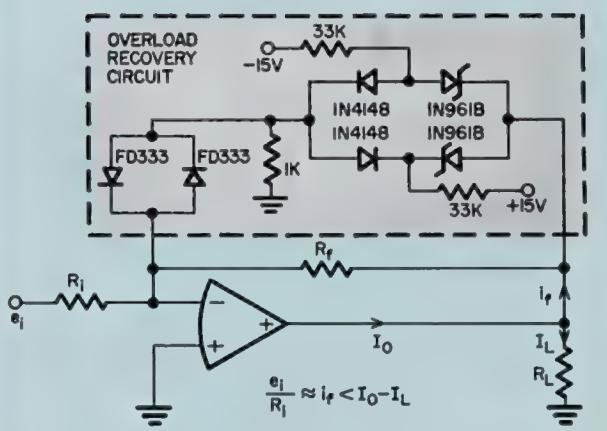


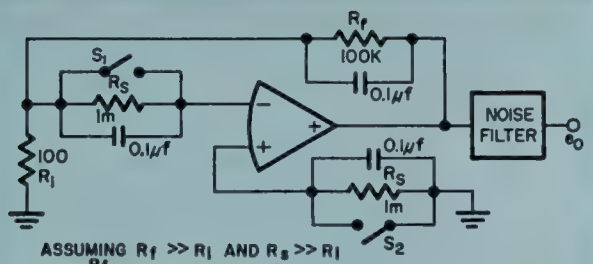
FIGURE 10. EXTERNAL CLAMP CIRCUIT FOR ±10 VOLTS

TEMPERATURE DRIFT

Offset voltage, bias current and difference current all change or "drift" from their initial values with temperature. By far this is the most important source of error in most applications. The temperature coefficients of these parameters, $\Delta e_{os}/\Delta T$, $\Delta i_b/\Delta T$ and $\Delta i_d/\Delta T$ are all defined as the average slope over a specified temperature range and are determined by subtracting the offset values at the end points of the temperature range and dividing by the temperature change. In general drift is a non-linear function of temperature and the slopes are greater at the extremes of temperature than around normal room ambient. The temperature drift coefficients are measured by the circuit of figure 11. The amplifier is used to boost its own low level input offset signal to a conveniently measurable voltage at the output. Gain is established by the ratio of R_f/R_i. The current sampling resistors, R_s, must be selected so that voltage drift is small compared to the drift due to difference current; that is $R_s \times \Delta i_d/\Delta T >> \Delta e_{os}/\Delta T$. Alternatively, voltage drift must be subtracted from the data for current drift.

One problem in using published voltage drift specifications is that this data applies only to static temperature conditions where the temperature of the module is assumed to be uniform. Voltage offset of most differential amplifiers is quite sensitive to thermal gradients, since drift performance depends on the cancellation of large offset in each transistor of the input differential pair. Therefore in environments where thermal gradients are present voltage offset may exceed that predictable from the drift coefficients. In this case where low drift over a narrow temperature range is critical, it is good practice to insulate or shield the amplifier to assure a uniform temperature. Bias current is not noticeably affected by thermal gradients and difference current, while affected, is far less sensitive to gradients than voltage offset.

Bias current and difference current for FET and varactor bridge amplifiers double each 10°C and therefore a linearized drift coefficient has little meaning except over a narrow operating temperature range.



ASSUMING $R_f >> R_1$ AND $R_s >> R_1$

$$e_o = -\frac{R_f}{R_1}\left[e_{os} \pm R_s(i_b^- - i_b^+)\right]$$

$$i_d = i_b^- - i_b^+$$

Parameter	Switch Position S1	S2	Output Voltage
e_{os}	Closed	Closed	$e_o = -(\frac{R_f}{R_1})e_{os}$
i_b^-	Open	Closed	$e_o = -(\frac{R_f}{R_1})R_s i_b^-$
i_b^+	Closed	Open	$e_o = -(\frac{R_f}{R_1})R_s i_b^+$
i_d	Open	Open	$e_o = -(\frac{R_f}{R_1})R_s i_d$

FIGURE 11. TEST CIRCUIT FOR OFFSET VOLTAGE, BIAS CURRENT AND DIFFERENCE CURRENT

SUPPLY VOLTAGE SENSITIVITY

Offset voltage, bias current and difference current will also change when supply voltage is varied. Usually errors due to this effect are negligible compared to temperature drift. Static or DC supply voltage coefficients, $\Delta e_{os}/\Delta V_s$, $\Delta i_b/\Delta V_s$, $\Delta i_d/\Delta V_s$ are measured with the circuit in figure 11 by varying supply voltages individually by ± 1 volt.

There is a common misconception that tracking power supplies whose plus and minus voltages change by the same amounts will improve supply voltage coupling. In general tracking supplies are of no benefit since the positive supply voltage coefficient is usually much larger than the negative supply voltage coefficient. Rejection of AC noise and ripple on the power supplies is not as good as static or DC rejection, but for almost all amplifiers AC rejection will be better than 1mV/V or 60dB over a wide range of frequencies.

DRIFT VS TIME

Offset voltage, bias current and difference current change with time as components age. Static data over long time periods is difficult to obtain because of the inherent time delays involved. But it is safe to say that the published time drift for amplifiers does not accumulate linearly. For example, voltage drift for a chopper stabilized amplifier (which by the way is by far the best amplifier type for long term stability) is usually quoted as $1\mu V$/day whereas cumulative drift over 30 days will usually not exceed $5\mu V$ nor $15\mu V$ in a year.

Long term voltage drift in differential input type amplifiers depends primarily on the aging of collector resistors in the input differential pair. The aging coefficient referred to the input is about $300\mu V/\%$ change of collector resistance. It is not unlikely that carbon composition resistors will age by 1 or 2% over a year resulting in an offset voltage change of 300 to $600\mu V$. The use of metal film resistors for the collector resistors will greatly improve long term stability to the point where base to emitter voltage aging is the determining factor. With metal film resistors, offset voltage for transistor amplifiers is about $100\mu V$/year while FET amplifiers will age somewhat more.

Long term bias current stability in differential input amplifiers again depends on resistor stability when internal initial current compensation is employed. In this case, multi-megohm carbon composition resistors are used (since large value metal film resistors are not available) to supply about 90% of the base bias current. If these resistors change by 1%, the specified initial bias current will change by about 9% which can be a substantial drift. Therefore one can conclude that amplifiers without internal initial current compensation will exhibit more stable bias current. Under these conditions long term bias current stability depends primarily on the stability of the transistor or FET devices which may be better than 1%.

INPUT IMPEDANCE

Differential input impedance, R_d, is defined as the impedance between the two input terminals, measured at 25°C, assuming that the error voltage, e_ε, is nulled or very near zero volts (see figure 1). For a single ended amplifier, R_d, is the input impedance since the plus input is grounded. To a first approximation, dynamic impedance can be represented by a capacitor, C_d, in parallel with R_d.

Differential input impedance is among the most difficult parameters to measure particularly for a high gain, high impedance type amplifier. In general this measurement can only be made under laboratory conditions by an experienced engineer with special fixtures to shield against noise pick up. For this reason most companies including Analog Devices rarely measure this parameter on a production line basis. Fortunately a precise knowledge of R_d is not required, since for most circuits, so long as R_d is large compared to the external feedback impedance, its value has little bearing on closed loop performance.

The circuits of figure 12 show in principle how R_d can be measured with enough attention to reducing noise. These circuits actually measure R_d in parallel with the negative input common mode impedance. However, common mode impedance is usually 10 to 100 times greater than R_d so that the error is negligible.

Common mode impedance, R_{cm}, is defined as the impedance between each input and ground or power supply common and is specified at 25°C. (See figure 1.) For most circuits common mode impedance on the negative input, R_{cm}^-, has little significance except for the capacitance which it adds to the summing junction. However, common mode impedance on the plus input, R_{cm}^+, sets the upper limit on closed loop input impedance for the non-inverting configuration. Dynamic impedance can be represented by a capacitor, C_{cm}, in parallel with R_{cm} which usually runs from 5 to 25 pf on the plus input.

The circuit of figure 13 can be used to measure R_{cm}^+ up to about 500M ohms. Use an oscillator frequency of 1 to 5Hz

and adjust R_s for 10% reduction at the output. Then $R_{cm}+ = 9R_s$. Above this impedance it is advisable to substitute a picoameter for the resistor R_s and to measure DC bias current as a function of common mode voltage.

Common mode impedance is a non-linear function of both temperature and common mode voltage. For FET amplifiers common mode impedance is reduced by a factor of two for each 10°C temperature rise.

As a function of common mode voltage, R_{cm} is defined as average impedance for a common mode voltage change from zero to $\pm E_{cm}$, that is, maximum common mode voltage. Incremental R_{cm} about some large common mode voltage may be considerably less than the specified average R_{cm}, especially for FET input amplifiers.

MAXIMUM VOLTAGE BETWEEN INPUTS

Under most operating conditions, feedback maintains the error voltage, e_ε, between inputs very near to zero volts. However, in some applications, such as voltage comparators, or where the input voltage exceeds the level required to saturate the output, the voltage between inputs can become large. E_d defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier. Placing parallel back to back diodes across the input terminals is one way to provide added protection for the amplifier.

MAXIMUM COMMON MODE VOLTAGE

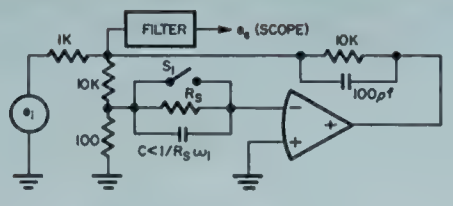
For differential input amplifiers, the voltage at both inputs can be raised above ground potential. Common mode voltage, e_{cm}, is defined as the voltage above ground at each input when both inputs are at the same voltage. E_{cm} is defined as the maximum peak common mode voltage at the input before clipping or excessive non-linearity is seen at the output. E_{cm} establishes the maximum input voltage for the voltage follower connection. (See figure 7.)

E_{cm} is measured with the circuit of figure 7 by increasing the peak input voltage (sinusoidal waveform) until distortion is seen on the scope (about 1 to 3%). The input signal frequency must be well below the full power response frequency, f_p, for the non-inverting input.

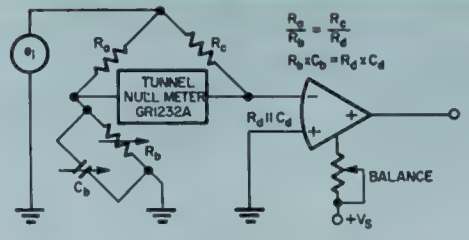
COMMON MODE REJECTION

An ideal operational amplifier responds only to the difference voltage between inputs ($e+ - e-$) and produces no output for a common mode voltage — that is when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, common mode input voltages are not entirely substracted at the output. If we refer the output common mode error voltage to the input (dividing by gain) and call this the input common mode error voltage, $e_{\varepsilon_{cm}}$, then common mode rejection (CMR) is defined as the ratio of common mode voltage to common mode error voltage. That is $CMR = e_{cm}/e_{\varepsilon_{cm}}$. CMR is sometimes expressed in dB in which case you take 20 times the log (base 10) of the ratio. Errors due to common mode rejection can be represented in the equivalent circuit of figure 1 by a voltage generator, $e_{\varepsilon_{cm}}$, in series with the input. Note that common mode error goes to zero when either input is grounded. Therefore the inverting configuration does not exhibit a common mode error since the plus input is grounded. Thus CMR is only a problem in the non-inverting and differential configurations where common mode voltage varies in direct proportion to the input signal. In this case $e_{\varepsilon_{cm}}$ is a basic measuring error which affects the overall circuit accuracy.

For example, if a 10 volt signal, e_i, were applied to the input of the circuit in Figure 14 common mode voltage, e_{cm}, is equal to the input voltage, e_i. This would cause a common mode voltage, $e_{\varepsilon_{cm}}$, of 2mV for an amplifier with 5,000 or 74dB CMR and thus a 0.02% measuring error.



SET e_i FOR 1 TO 5 Hz, INCREASE R_s UNTIL OPENING S_1 INCREASE e_o BY FACTOR OF 2. THEN $R_s = R_d$



BALANCE DC OUTPUT REDUCE e_i TO SMALLEST POSSIBLE VOLTAGE AND FREQUENCY

FIGURE 12. DIFFERENTIAL IMPEDANCE TEST CIRCUITS

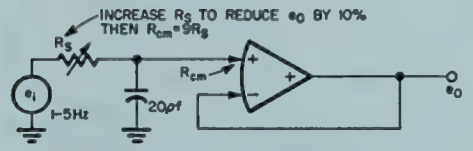


FIGURE 13. COMMON MODE IMPEDANCE TEST CIRCUIT

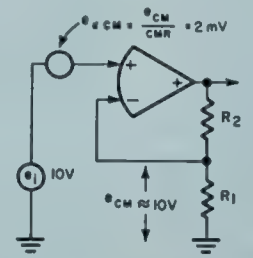


FIGURE 14. ILLUSTRATION OF COMMON MODE VOLTAGE

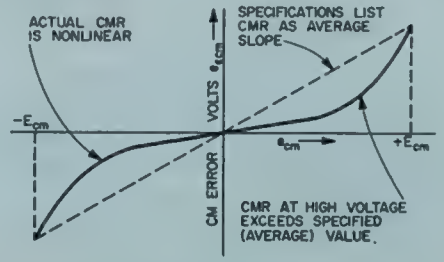


FIGURE 15. CM ERROR VS CM VOLTAGE

Operational Integrators

By RAY STATA, *Vice President and Co-founder Analog Devices, Inc.*

Modern solid state operational amplifiers make remarkably good integrators. Almost any degree of accuracy can be achieved depending on the choice of the amplifier and the feedback capacitor. A great deal of literature exists† which discusses integrator error in analog computers and this subject will not be covered here. But we shall review the non-ideal characteristics of operational amplifiers (and to some extent capacitors) which limit the performance of integrators in instrumentation circuits. This we hope will help the reader make a better choice of amplifiers for his particular application.

†Korn and Korn, *Electronic Analog and Hybrid Computers* — McGraw Hill.

An ideal operational amplifier for integrator applications would have infinite open loop gain and input impedance and zero offset voltage and current (that is, $e_o = o$, when $e_i = o$). For this case, Figure 1 shows the characteristics of an ideal integrator.

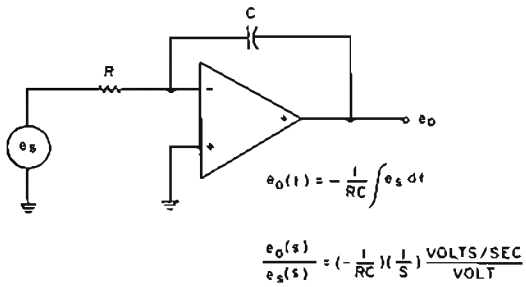


Figure 1. Ideal Operational Integrator

The gain (or characteristics time) of the circuit is given by 1/RC, which is to say that the output will change by (1/RC) volts/sec for each volt of input signal. The input impedance as viewed from the source voltage, e_s, is determined by the value for R.

OFFSET AND DRIFT ERRORS

By far the greatest source of error in integrators is due to offset and drift of the amplifier. An equivalent circuit is given in Figure 2 from which we can predict the errors due to offset. For the moment we shall assume that open loop gain, A, and open loop input impedance, R_d, are infinite.

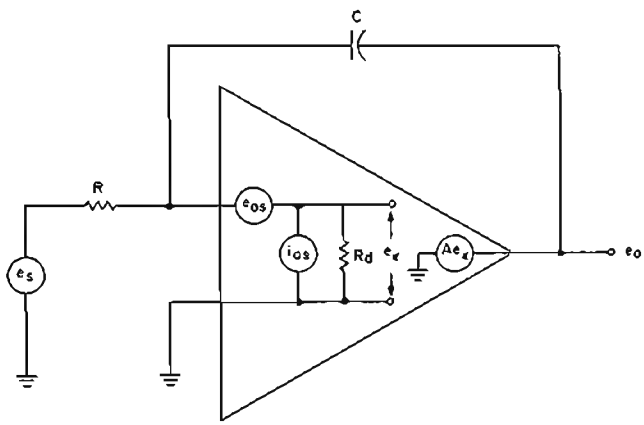


Figure 2. Equivalent Circuit for Integrator

$$e_{os} = \underset{\substack{\mu V \\ \text{at} \\ 25°C}}{E_{os}} + \underbrace{\frac{\Delta e_{os}}{\Delta T}}_{\mu V/°C}\Delta T + \underbrace{\frac{\Delta e_{os}}{\Delta V_s}}_{\mu V/\%}\Delta V_s + \underbrace{\frac{\Delta e_{os}}{\Delta t}}_{\mu V/day}\Delta t$$

$$i_{os} = \underset{\substack{\text{pa} \\ \text{at} \\ 25°C}}{I_{os}} + \underbrace{\frac{\Delta i_{os}}{\Delta T}}_{pa/°C}\Delta T + \underbrace{\frac{\Delta i_{os}}{\Delta V_s}}_{pa/\%}\Delta V_s + \underbrace{\frac{\Delta i_{os}}{\Delta t}}_{pa/day}\Delta t$$

As shown the offset voltage, e_{os}, and the offset current, i_{os}, can be calculated for any temperature, supply voltage and time period from the drift coefficients of the amplifier. It is usually possible to adjust the initial offset voltage and current, E_{os} and I_{os}, to zero by some biasing network.

The simplest way to analyze offset errors is to refer them to the source voltage as shown in Figure 3. In this case offset current is multiplied by R and becomes a voltage source. When viewed at the

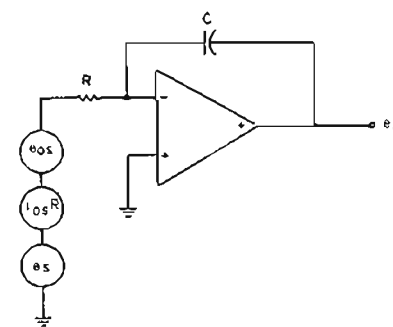


Figure 3. Offsets Referred to the Input

input, the offsets cannot be distinguished from the input signal and hence introduce a basic error in the integration of the signal. The percentage error would be, % error $= (e_{os} + i_{os}R)\ 100/\bar{e}_s$, where $\bar{e}_s$ is

the time average of the input signal over the integration period. Notice that R should be as small as possible to minimize offset errors for a given amplifier. But remember that R also sets the input impedance for the integrator.

When referred to the input, the analysis of offset errors is not much different for an integrator than for an inverting DC amplifier. More detailed information is given on this subject in an Analog Devices' application note entitled "Part IV, Offset and Drift in Operational Amplifiers."

In some applications it is necessary to refer the offset error to the output in order to derive meaningful results. In this case the output error is a drift rate which is given by,

$$\frac{de_o}{dt} = \frac{e_{os} + Ri_{os}}{RC} = \frac{e_{os}}{RC} + \frac{i_{os}}{C}$$

Again, we see that output drift rate is minimized by using the smallest value for R and the largest value for C. This follows since the drift rate due to offset voltage is fixed by the gain of the circuit (1/RC) whereas the drift rate due to offset current is reduced by using a larger C.

The practical limits on the choice of R and C are as follows:

1. Source impedance sets a minimum value on input impedance which is equal to R.
2. The physical size, price and quality are all serious problems in using large value capacitors particularly when greater than 1 to 5μf.

For differential input amplifiers, the error due to offset current is generally reduced by balancing the impedance as seen from each input to ground. For the circuit in Figure 3 this would amount to inserting a resistor from the plus input to ground equal to R. Due to the input symmetry of a differential amplifier, offset current at each input tends to be equal and tends to track with temperature and thus the drift error is reduced by balancing impedances.

ERRORS DUE TO FINITE GAIN, INPUT IMPEDANCE AND BANDWIDTH

The open loop gain response for most operational amplifiers can be represented by the graph in Figure 4. If we go back to Figure 2 and assume that the amplifier has to gain response of Figure 4 and an open loop input impedance, R_d, then the exact expression for integrator gain would be:

$$\frac{e_o(s)}{e_i(s)} = \underbrace{\left[\frac{-1}{RCs}\right]}_{\text{ideal}} \underbrace{\left[\frac{1}{1+\left(\frac{1+T_o s}{A_o}\right)\left(1+\frac{1}{R_p Cs}\right)}\right]}_{\text{error due to finite gain and bandwidth}} \quad (1)$$

where $R_p = R_d R / R_d + R$ (parallel sum)

Equation (1) can be simplified if we assume that $A_o >> 1$ (a very safe bet):

$$\frac{e_o(s)}{e_i(s)} = \left[\frac{-1}{RCs}\right]\left[\frac{1}{1+\frac{s}{\omega_t}+\frac{1}{A_o R_p Cs}}\right] \text{ for } A_o >> 1 \quad (2)$$

where $\omega_t \approx A_o/T_o$ is the amplifier unity gain bandwidth.

HIGH FREQUENCY ERRORS DUE TO FINITE BANDWIDTH

Finite amplifier bandwidth imposes some limitation on the ability of the integrator to respond to instantaneous input changes. The transient behavior at t = o can be predicted by examining the behavior of equation (2) at high frequencies. In this case equation (2) becomes:

$$\frac{e_o(s)}{e_i(s)} = \frac{-1}{RCs}\left(\frac{1}{1+s/\omega_t}\right) \text{ for } s >> \frac{1}{A_o R_p C} \quad (3)$$

This is the equation for an ideal integrator except for a time lag which is inversely proportional to the unity gain bandwidth, ω_t. To illustrate the error due to finite bandwidth, consider the response of (3) to a step function input as given by (4) and Figure 5.

$$e_o(t) \approx \frac{1}{RC}\left(t - 1/\omega_t\right) \text{ for } e_i(t) = -\mu_{-1}(t) \quad (4)$$

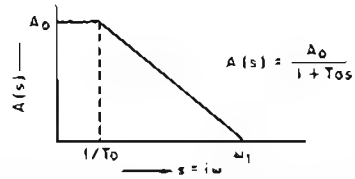


Figure 4. Typical Open Loop Gain Response

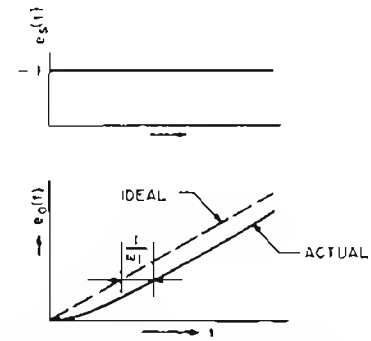


Figure 5. Step Response of Integrator at t = o

Note that the time lag depends only on amplifier open loop bandwidth, ω_1, and is independent of the values for R and C.

LOW FREQUENCY ERRORS DUE TO FINITE GAIN

The behavior of an integrator over long time periods can be predicted by the low frequency response of the circuit. In this case, where $s << \omega_1$, equation (2) becomes:

$$\frac{e_o(s)}{e_i(s)} = \left[\frac{-1}{RCs}\right]\left[\frac{1}{1+\frac{1}{A_oR_pCs}}\right] = -\frac{A_oR_p/R}{1+A_oR_pCs} \qquad (5)$$

Insight is gained into the operation of integrators at low frequencies by realizing that (5) is equivalent to the response of an ideal integrator with an infinite gain and input impedance amplifier, but with a feedback resistor A_oR_p in parallel with the feedback capacitor as shown in Figure 6.

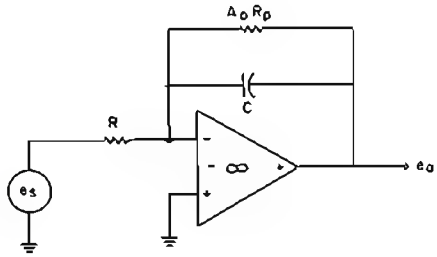


Figure 6. Integrator Low Frequency Equivalent Circuit

To illustrate more clearly the effect of low frequency errors, consider the response of (5) to a step function input as given by (6) and Figure 7.

$$e_o(t) = \frac{R_pA_o}{R}(1-e^{-t/A_oR_pC}), \text{ for } e_i(t) = -\mu_{-1}(t) \qquad (6)$$

Expanding (6) into a power series we have:

$$e_o(t) = \frac{t}{RC} - \frac{t^2}{2A_o(R_pC)(RC)} + - - -$$

The first term in this series is the response for an ideal integrator, while the second term is the principle error component which grows as the square of time.

In summary low frequency integrator errors are inversely proportional to finite open loop voltage

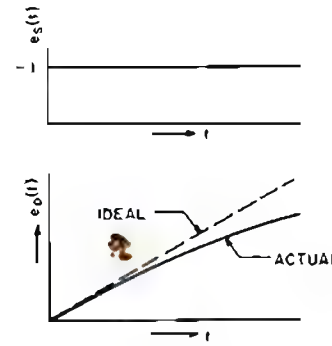


Figure 7. Step Response Showing Low Frequency Error Due to Finite Gain

gain. This follows from the fact that with finite gain the error voltage is not zero, as usually assumed, which tends to reduce input current as the output grows.

INTEGRATOR HOLDS ERRORS

One important use of integrator circuits is to precisely remember or hold a voltage potential. Finite amplifier gain causes a fixed integrator output voltage to droop.

Intuitively it is apparent from Figure 6 that the effective leakage resistance, A_oR_p, due to finite voltage gain and input impedance tends to discharge any fixed voltage stored across the feedback capacitor.

To develop a quantitative expression for this error, assume that the circuit in Figure 6 has the initial condition $e(o) = E_o$ and that $e_i = o$. In this case, the output voltage is simply:

$$e_o(t) = E_oe^{-t/A_oR_pC}$$

By expansion this becomes:

$$e_o(t) = E_o - E_o\left[\frac{t}{A_oR_pC} - \frac{t^2}{2(A_oR_pC)^2} + - - -\right] \qquad (7)$$

The first item of (7) is the output of an ideal integrator, while the terms in the brackets represent the errors due to finite gain. Figure 8 shows integrator hold error.

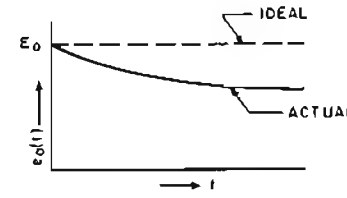


Figure 8. Integrator Hold Error

It is interesting to note that minimum error is obtained in hold operation when the input resistor is open circuited rather than short circuited. In this case the equivalent circuit is shown in Figure 9.

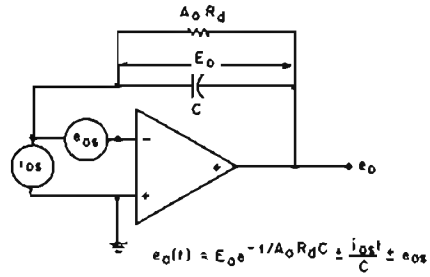


Figure 9. Hold Circuit with Input Open

Note that the equivalent feedback leakage resistor is determined only by the open loop input impedance and gain (A_oR_d). Further, the output drift rate is determined only by the offset current. Voltage offset appears at the output as a fixed offset.

FEEDBACK CAPACITOR

The performance of operational amplifiers have now reached the point where the quality of the feedback capacitor can limit the accuracy in the most precise applications. Therefore a brief discussion of capacitor limitations will be helpful in precise integrator design.

The chart in Figure 10 shows the salient characteristics for various types of high quality capacitors. This data was compiled with the assistance of Southern Electronics Corporation, Burbank, California, a capacitor manufacture who specializes in high quality capacitors for integrator applications. An application note from this company entitled "Capacitor Talk" gives more information on the interpretation of capacitor specifications.

In analog computers where scale factor accuracy is important it is common practice to enclose the feedback capacitor in a temperature controlled oven. In this case long term stability of capacitance value for polystyrene and mylar capacitors is about 0.1% per year.

Insulation Resistance — One important limitation for integrator capacitors is insulation or leakage resistance. The specification used to define this limitation usually is expressed in megohms - microfarads, which is equivalent to the time in seconds for a fixed voltage stored on the capacitor to discharge to 63% of its initial value. As a general rule the maximum insulation resistance is about two times the value for a one microfarad capacitor, which establishes the limit for insulation resistance of small capacitor values.

Dielectric	Mylar	Metalized Mylar	Poly-carbonate	Metalized Poly-carbonate	Polystyrene	Teflon	Metalized Teflon
Temperature Range							
Hi Temp (°C)	+125	+125	+125	+125	+85	+200	+200
Lo Temp (°C)	−65	−65	−65	−65	−65	−65	−65
Temperature Coefficient							
−65°C to 25°C (%)	−6	−6	−1.5	−1.5	+0.9	+1.9	+ 0.5
25°C to Hi Temp (%)	+12	+12	±0.5	± 0.5	−0.6	−3.7	−1.0
Dielectric Absorption							
% @ 25°C	0.1	0.1	.05	.05	.02	.01	.02
Dissipation Factor							
@25°C (%)	0.3	0.5	0.1	0.2	0.02	0.01	0.1
@ Hi Temp (%)	1.2	1.7	0.07	0.6	0.04	0.02	0.2
Insulation Resistance							
@ 25°C (MΩ-μf)	$2x10^5$	$5x10^4$	$4x10^5$	$2x10^5$	$1x10^6$	$1x10^6$	$5x10^5$
@ Hi Temp (MΩ-μf)	$3x10^2$	$1x10^2$	$1.5x10^4$	$15x10^2$	$7x10^4$	$1x10^5$	$2.5x10^4$
Approximate Size for 50Vdc							
cubic inch/μf (uncased)	.12	0.06	.19	0.09	.44	1.1	0.39

Figure 10. Comparison of Capacitor Specifications

The effect of insulation resistance can be represented in Figures 6 and 9 as another resistance in parallel with A_oR_p or A_oR_d and the issuing equations are modified accordingly. The insulation resistance of the very best capacitors is about 10^{12} ohms. By comparison a chopper stabilized operational amplifier will have open loop input impedance, R_d, of 10^6 ohms and open loop gain, A_o, of 10^8 giving an equivalent resistance of 10^{14}. Even an inexpensive differential amplifier will have equivalent leakage resistance of 10^{10} to 10^{11} ohms. Thus we see that the capacitor and not the amplifier usually sets the limit on performance in this regard.

Dielectric Absorption — One of the single most important dynamic errors of integration is due to dielectric absorption. This error results from the fact that when a capacitor is charged or discharged not all of the dielectric polarization takes place immediately. Consequently there can be an appreciable residual voltage with a relatively long time constant. The specification given for this parameter is the residual voltage expressed as a percentage of the applied voltage measured approximately one second after the capacitor is discharged. Polystyrene and teflon are mostly used for precision integrators since these materials have small but measurable errors due to dielectric absorption. For additional information on analyzing this source of error you should refer to "An Analysis of Certain Errors in Electronic Differential Analyzers II—Capacitor Dielectric Absorption," P. C. Dow, IRE Trans. on Electronic Computers, Vol. EC-7, pp.17-22, March, 1958.

Dissipation Factor, which is related to dielectric absorption, can be termed the sum total of all the losses in the capacitor and is expressed as the percentage ratio of the effective series resistance to the reactive capacitance, or as the tangent of the loss angle. Dissipation factor is important in AC integrators or in analog computers where repetitive integration is performed.

LEAKAGE RESISTANCE

In the highest performance integrators, leakage resistance to the summing junction or across the feedback capacitor can play a large role in the attainable performance. It is extremely important to shield the summing junction and its leads from leakage paths to potentials other than ground. For example, offset current, which is one of the principle limitations to good integrator performance, in a good chopper amplifier is about 10^{-11} amps. The insulation resistance required to keep the leakage current from the 15VDC supply voltage less than 10^{-11} amp would have to be greater than one million megohms. The insulation resistance of most wire and connectors fall short of this requirement. However, by properly shielding the summing junction and its leads, leakage currents from active sources are shunted to ground, effectively creating extremely high insulation resistance from these potentials to the summing junction.

By the same token leakage resistance of the clamping circuits across the feedback capacitor used to reset the integrator should not be overlooked when calculating the effective leakage of a feedback capacitor. For example, the leakage resistance of a computer grade capacitor is typically 10^{12} ohms, which may be negligible compared to the leakage resistance of a relay or a solid state switch.

AC INTEGRATORS

In some applications it may be desirable to integrate AC signals over a reasonably long time and it may not be possible to reset the output to zero periodically. In this case the DC offset problem can be alleviated in part by bounding the DC closed loop gain as shown in Figure 11.

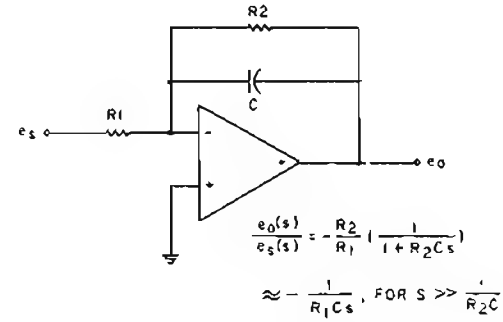


Figure 11. AC Integrator

The closed loop response for this circuit is shown in Figure 12.

For frequencies greater than $1/R_2C$ the response approaches that of an ideal integrator with gain of $1/R_1C$. For example, for signal frequencies, ω_s, a decade away from the corner frequency, $1/R_2C$, the gain error is only .5%.

The advantage of bounding the DC gain with R_2 is that the amplifier output will not drift into saturation. Instead the output will assume a DC value of $e_o = -R_2/R_1 (e_{os} + R_{1}i_{os})$. This output will limit the dynamic range for AC output signals; but, by choosing an amplifier with sufficiently low offsets, satisfactory operation can be obtained for many AC integrator applications.

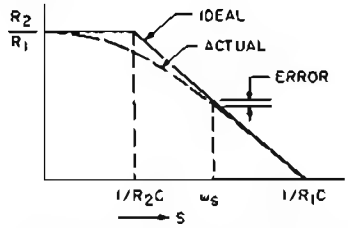


Figure 12. Gain Response for AC Integrator

For integration of very low frequency AC signals, the DC gain requirements of the previous circuit are so large as to cause saturation of the output. In this case the following circuit allows the DC gain to be reduced.

The lowest frequency which can be accurately integrated is limited by the size for C_2. The general expression for the corner frequencies ω_1 and ω_2 are rather complex and as a practical matter can only be determined by trial and error calculations. The lowest signal frequency, ω_s, should be at least ten times greater than ω_2.

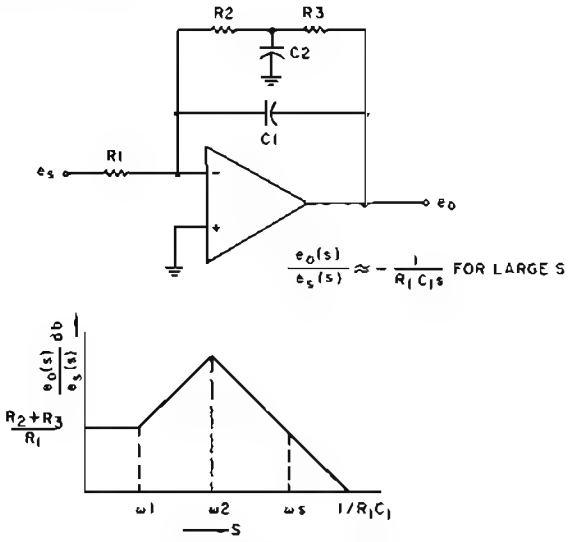


Figure 13. Low Frequency AC Integrator

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OPEN LOOP GAIN

Open loop gain, A, is defined as the ratio of output voltage to error voltage between inputs as shown in Figure 1. Usually gain is specified only at DC, but in

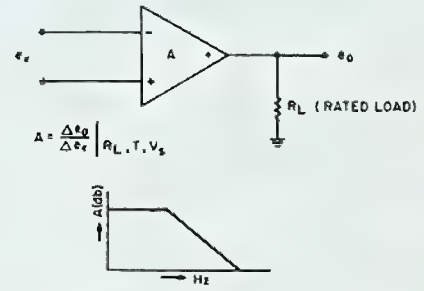

Figure 1. Definition of Open Loop Gain

many applications such as AC amplifiers the frequency dependence of gain is also important. Open loop gain changes with load impedance (R_L), ambient temperature and supply voltage. As a rule, open loop gain will not change more than a factor of 10 between rated load and no load conditions. Most operational amplifiers have a positive gain temperature coefficient of about 0.5 to 1%/°C and gain changes with supply voltage at about 2%/%. Analog Devices specifies all open loop gains at rated load, 25°C and rated supply voltages.

TEST CIRCUIT

A practical circuit for measuring open loop gain over a range of frequencies is shown in Figure 2. The voltage divider on the negative input boosts the sen-

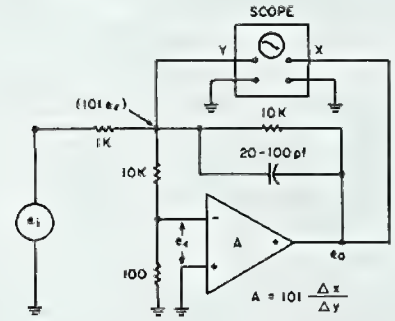

Figure 2. Open Loop Gain Test Circuit

sitivity of the error voltage by 100 times which makes it possible to measure gains of several million. At low frequencies open loop gain is constant so that DC gain can be measured by a low frequency signal (about 5Hz). The voltage divider may not be necessary for low gain amplifiers (below 20,000) and it is not recommended for measuring gain at high frequencies where open loop gain is less. At very best, noise pickup is a problem for measuring high

GLOSSARY OF DEFINITIONS

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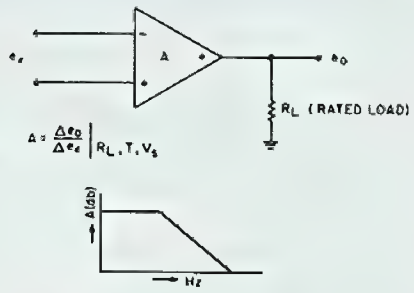

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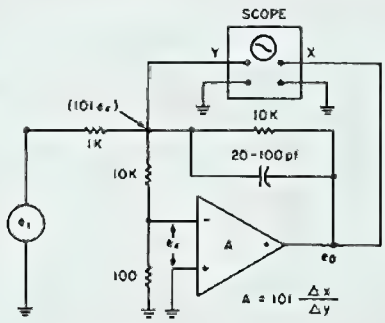

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At high frequencies the amplitude of the output voltage must be reduced to avoid exceeding the slewing rate of the amplifier. For this reason the output voltage should be adjusted, so that e_o (peak) < Slew Rate/ω_i.

SIGNIFICANCE OF GAIN

Operational amplifiers are rarely used open loop. Instead negative feedback is used around the amplifier to improve the accuracy of the circuit. This introduces a second term, closed loop gain (G), which is defined as the gain of the circuit with feedback. The simple inverting amplifier in Figure 3 illustrates this point.

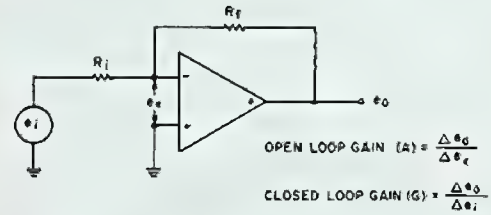


Figure 3. Closed Loop Circuit

Linearity, gain stability, output impedance and gain accuracy are all improved by the amount of feedback. Figure 4 graphically illustrates the relation between open loop gain and closed loop gain.

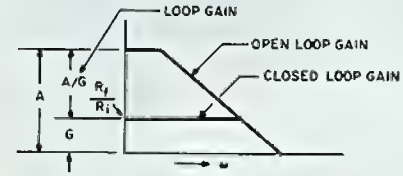
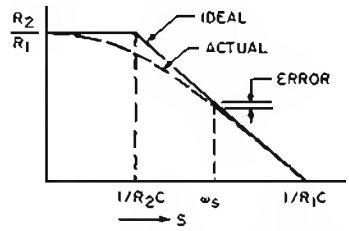


Figure 4. Determination of Loop Gain

The excess of open loop gain over closed loop gain is called loop gain. (Subtraction of dB is equivalent to arithmetic division.) The improvement of open loop performance due to feedback is directly proportional to loop gain. As a general rule for moderate accuracy, open loop gain should be 100 times greater than the closed loop gain at the frequency, or frequencies, of interest (that is loop gain = 100). For higher accuracy, loop gain should be 1000 or more. To illustrate, we recall that open loop gain stability for most operational amplifiers is about 1%/°C. With loop gain of 100, closed loop gain stability would be 100 times better or 0.01%/°C. Likewise, closed loop output impedance would be 100 times less than open loop output impedance with a loop gain of 100.



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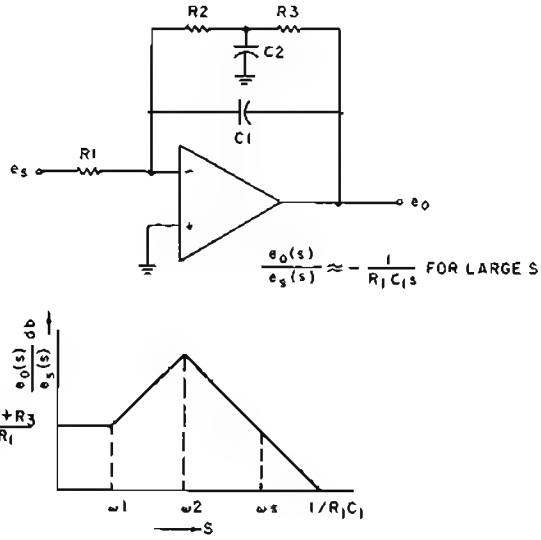

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Discusses advantages to be gained by using a floating power supply in op amp circuits particularly with chopper stabilized amplifiers. (6 pages)

Differential Amplification
Zeltex, Inc.
Concord, California

A thorough treatment of configurations for obtaining differential amplification from op amps. (11 pages)

Surveying the Analog IC
Electronic Design News, *February 1967*
3375 S. Bannock Street
Englewood, Colorado

A magazine survey article on what's available in integrated circuit op amps. (5 pages)

Differentiator Noise
Electronic Design, *June 21, 1966*
850 Third Avenue
New York, New York

A good starting point for analyzing noise in differentiators. Noise transfer function given for a variety of circuit configurations. (3 pages)

Source and Load Impedance: Effects on Closed, Loop Characteristics
Electro-Technology, *September 1966*
205 East 42nd Street
New York, New York

Exact equations are given for the effects of source and load impedance in op amp circuits. Article can save you a great deal of laborious effort in derivations. (8 pages)

Electronic Analog and Hybrid Computers, Korn & Korn, 1964
McGraw Hill Book Co.
330 West 42nd Street
New York, New York

A textbook mainly on analog computers, but with a great deal of useful information on op amp circuits. (584 pages)

Printed in U.S.A.

ANALOG DEVICES

APPLICATIONS MANUAL

Models 201, 202, 203 & 210
Chopper Stabilized Operational Amplifiers

Ray Stata, Vice President
Analog Devices, Inc., Cambridge, Mass.
1967

1.0 INTRODUCTION

1.1 Description

Analog Devices ' 200 Series chopper stabilized amplifiers utilize a low frequency AC amplifier, modulator, and demodulator to improve the drift characteristics of a conventional differential operational amplifier while retaining the wideband characteristics of the unstabilized amplifier (with the exception of differential inputs). The modulator (chopper) and demodulator are completely solid state, driven by an internal solid state chopper drive. A high speed overload recovery circuit is included as standard on all amplifiers. Outputs are completely short circuit protected.

The philosophy of operation consists of dividing the incoming frequency spectrum into two parts, such that all frequencies above a few cycles per second are amplified in a conventional manner by the main channel, while the very low frequency input signals are chopped, amplified by an AC amplifier, and demodulated before being applied to the main channel of the amplifier. This effectively divides the drift of the main channel amplifier (referred to the input) by the gain of the chopper amplifier, with the result that the predominant contributions to drift are those of the low level modulator.

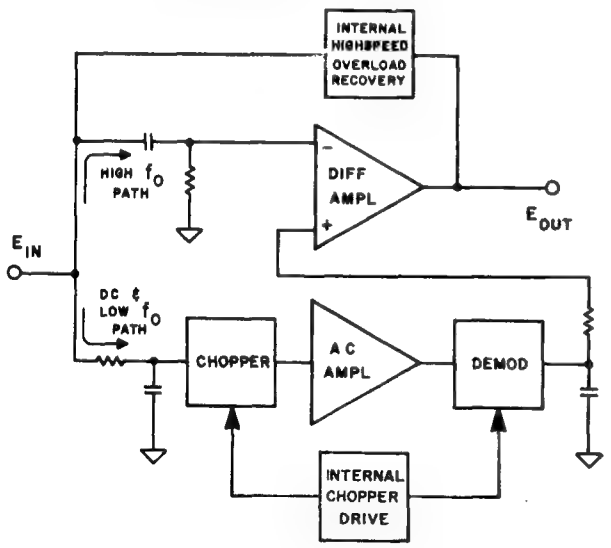


FIGURE 1 - CHOPPER STABILIZED AMPLIFIER BLOCK DIAGRAM

1.2 Basic Operation

The block diagram is shown in figure 1. DC and very low frequency components of the input signal are directed by a low pass filter to the chopper, are chopped, amplified, demodulated, filtered and applied to one input of the main channel. Higher frequency input signals are routed by the high pass filter directly to the main channel. The two frequency spectrums are re-combined by summing at the different inputs of the main channel. Proper phase relationship of the low frequency signals is accomplished by a phase reversal through the AC section and then by a second phase reversal via the (+) input of the main channel to be in phase with the higher frequency components applied directly to the (-) input of the main channel.

1.3 Chopper Stabilized vs. Differential Op Amps

With recent improvements in unstabilized operational amplifiers, a discussion of the advantages of chopper stabilized amplifiers may be of value. Voltage drift of unstabilized units is available to 3μV/°C and reported to be possible to less than 1μV/°C. This does not compare badly with drifts of 0.2μV/°C to 1.0μV/°C for stabilized amplifiers. However, offset current and current drift are much better in stabilized amplifiers; 50pA and .5pA/°C versus 1nA and 50pA/°C and only over a limited temperature range at that for unstabilized amplifiers.

Less obvious advantages of stabilized amplifiers are the short time required for warm up to within specifications, and the immunity to thermal gradients. Differential amplifiers have a warm up period of about 20 minutes, during which time initial offset voltage may change by several hundred microvolts. There is also great sensitivity to externally generated thermal gradients and in some cases internally generated gradients due to changing load conditions. These thermal drifts may be well in excess of those produced by changes in ambient temperature, particularly when operated over a narrow range of ambient temperatures.

A further advantage of stabilized amplifiers is that long term offset stability at constant temperature is excellent-as little as 10 μV over a several month period-while initial offset voltage of differential, unstabilized amplifiers may drift several hundred microvolts over the same period.

1.4 Special Features

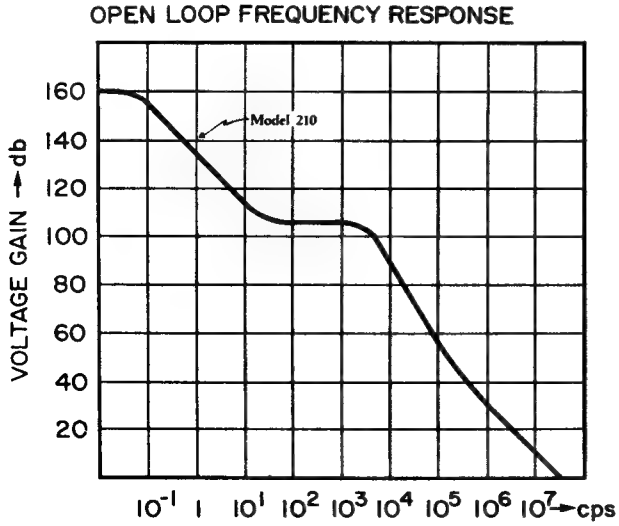
Special features of Analog Devices' 200 Series amplifiers include:

1. An internal chopper drive that eliminates an externally generated 60 Hz drive signal and the AC noise pick up usually accompanying this.
2. An integral zener, resistor, diode clamping network that keeps the amplifier from saturation and returns the output to the linear region after an input overload in less than a microsecond.
3. Output is short circuit proof with short circuit current limited to about 100 ma for all models including Model 201.

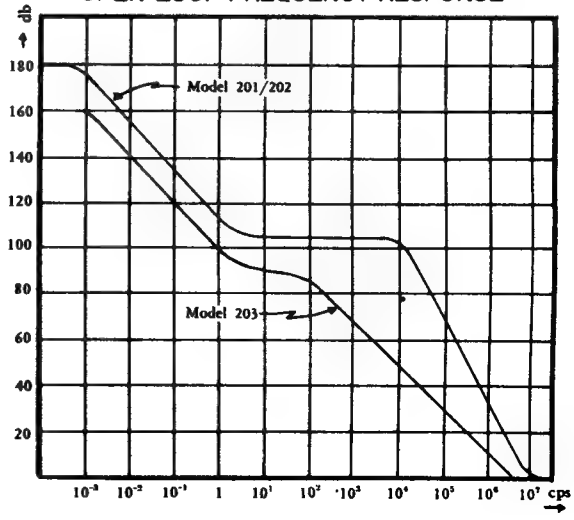
2.0 SELECTION GUIDE

Specifications (typical at 25°C and ±15VDC unless otherwise noted)	Model 201	Model 202	Model 203	Model 210
OPEN LOOP GAIN, dc, rated load	10^9	10^9	10^8	10^8
RATED OUTPUT				
Voltage, p to p, min.	±11 V	±11 V	±11 V	±10 V
Current, min.	100ma	20 ma	20 ma	20 ma
FREQUENCY RESPONSE				
Unity Gain, Small Signal	10mc	10 mc	2 mc	20 mc
Full Power Response	500KC	500 KC	20 KC	500 KC
Slewing Rate	30V/μsec	30V/μsec	1.2V/μsec	100V/ μsec
Overload Recovery	0.5μsec	0.5μsec	5μsec	0.2μsec
INPUT OFFSET VOLTAGE				
Initial Offset, 25°C, max.	±20μV	±20μV	±20μV	±100μV
Average vs. Temp. (-25 to 75°C) max.	0.2μV/°C	0.2μV/°C	0.2μV/°C	--
(+10 to 85°C) max.	--	--	--	1μV/°C
(-25 to 10°C) max.	--	--	--	2μV/°C
vs. Supply Voltage	0.4μV/%	0.4μV/%	0.4μV/%	10μV/%
vs. Time	1μV/day	1μV/day	1μV/day	1μV/day
INPUT OFFSET CURRENT				
Initial Offset, 25°C, max.	±50pa	±50pa	±50pa	±100pa
Average vs. Temp. (-25 to 75°C) max.	0.5pa/°C	0.5pa/°C	0.5pa/° C	--
(-25 to 85°C) max.	--	--	--	2pa/°C
vs. Supply Voltage	1pa/%	1pa/%	1pa/%	10pa/%
INPUT CHARACTERISTICS				
Input Impedance, dc, open loop	220KΩ	220KΩ	220KΩ	500KΩ
Voltage Noise, DC to 1cps, p to p	25 μV	25μV	10μV	5μV
5cps to 50KC, rms	10 μV	10μV	10μV	10μV
Current Noise, DC to 1cps, p to p	20 pa	20pa	10pa	10pa
POWER SUPPLY				
Voltage	± 15 to 16 VDC	± 15 to 16 VDC	± 15 to 16 VDC	± 15 to 16 VDC
Current, quiescent	+ 15, - 25 ma	+ 13, - 20 ma	+ 13, -20 ma	+ 40 , -10 ma
TEMPERATURE RANGE				
Specifications	-25 to 75°C	-25 to 75°C	-25 to 75°C	-25 to 85°C
Operating	-40 to 75°C	-40 to 75°C	-40 to 75°C	-40 to 85°C
Storage	-55 to 75°C	-55 to 75°C	-55 to 75°C	-55 to 100°C
PRICE (1-9)	$270.	$235.	$215.	$157.
(10-24)	$256.	$224.	$205.	$148.

OPEN LOOP FREQUENCY RESPONSE



OPEN LOOP FREQUENCY RESPONSE



3.0 AMPLIFIER INSTALLATION & APPLICATION CONSIDERATIONS

3.1 Pin Connections

The pin configuration and wiring diagrams shown in figures 2 and 3 indicate how the amplifier should be connected for proper operation. Note that the input return terminal must be externally connected to power supply common unless an external balance pot is required (see below). To prevent ground loops, a separate wire should go directly from the input return to power supply common. The small dot in the

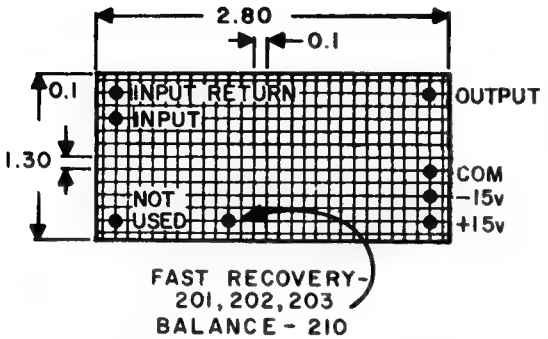


FIGURE 2 - PIN LAYOUT
(BOTTOM VIEW)

bottom corner of the amplifier triangle symbol denotes a connection to the power supply common. The input return for all figures (after figure 4) is implied to be connected externally to the power supply common. Where the fast overload recovery feature is desirable on Models 201, 202, and 203, the fast overload terminal must be externally shorted to the output terminal. Model 210 has the fast overload recovery circuit always operative (internally connected):

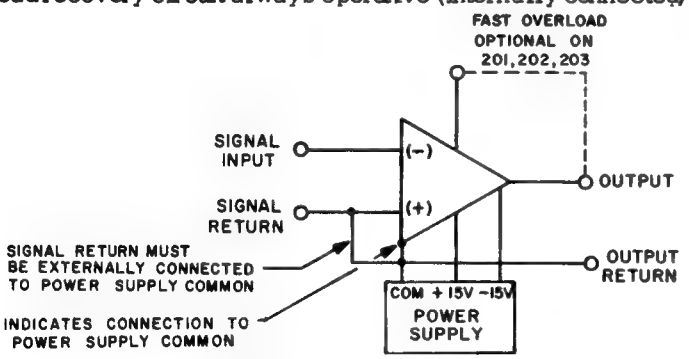


FIGURE 3 - CONNECTIONS

The amplifiers can be damaged by applying incorrect polarity of supply voltage. Be sure polarities are correct.

Remember that the exceptionally low drift and input current specification can be degraded by improper external wiring. Leakage resistance from the summing junction to an external voltage potential is particularly critical. For example, a leakage resistance of 10^{12}ohms between the summing junction and the 15VDC supply voltage results in 15pA input current, which is greater than the typical initial offset current of the amplifier. For critical applications such as high quality integrators, leads to the summing junction should be isolated from external voltage potentials by ground potential shielding. Moreover, thermocouple voltages can generate offset voltage drift comparable to that of the amplifier and precautions should be taken to minimize this source of offset potential.

3.2 External Zero Offset Adjustments

Typical initial offset voltage on the 201, 202, and 203 is ±10μV with a maximum specification of ±20μV. In most circuits such low offset does not require an external balance adjustment. However, in critical applications the circuit in figure 4 can be used to zero the amplifier. The range of adjustment for the resistor values given is about

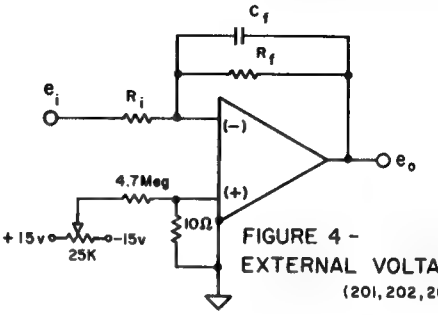


FIGURE 4 - EXTERNAL VOLTAGE BALANCE (201, 202, 203)

±30 μV. The 4.7 megohm resistor can be decreased for a greater range adjustment where it is desirable to zero suppress an external offset voltage. The input return should never be raised above a few millivolts unless the factory is consulted for the possible effects on other operating specifications, moreover, impedances greater than 100 ohms should never be used in the input return lead. Notice that the stability of the ±15VDC bias voltages and of the voltage divider resistors are not particularly critical since, for example, a 1% change of 30μV is only 0.3μV.

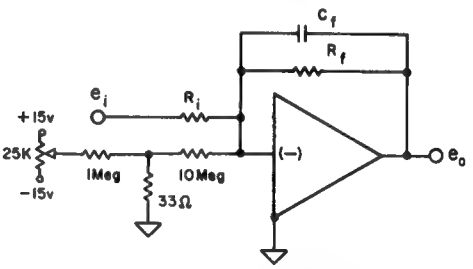


FIGURE 5 - EXTERNAL CURRENT BALANCE

For precision integrator or low offset current applications, the initial offset current can be zeroed with the circuit shown in figure 5 as an alternative to the voltage biasing of figure 4. The adjustment range of the bias circuit in figure 5 is ±50pA.

For a fixed source impedance, voltage or current biasing have an equivalent effect and either technique can be used to zero both initial voltage and current offsets. However, for a change source impedance in critical applications, as in the case of opening and shorting the input or in multiplexing the input to various source impedances, then both voltage and current biasing must be used to zero offset voltage and current independently.

Model 210 has a maximum initial offset voltage of ±100μV but requires only an external 50K pot connected to the balance terminal for zeroing. If initial voltage zero is not required, the balance terminal of the amplifier should be left open. The circuit of figure 5 may also be used with the 210 to zero initial offset current if desired, except the adjustment range should be increased to ±100pA by increasing the 33Ω resistor to 68Ω.

3.3 Single Ended Input

The 200 Series, like most chopper stabilized operational amplifiers, have single ended (inverting only) inputs. This means that one side of the input signal must be common to the power supply ground and the output ground.

Special circuitry is required to perform non-inverting and differential input amplification. Refer to paragraphs 5.3 and 5.4 for circuits and considerations.

3.4 Closed Loop Stability

The high frequency performance of Models 201, 202, and 210 is characterized by a useful small signal bandwidth of up to 10mc, slewing rates of 30 to 100 V/μsec and open loop gain greater than 60db at 100KC. Note that gain bandwidth product at unity gain is 10mc, but increases for a closed loop gain of 100 to 80mc. These specifications are achieved in part by internal phase compensation networks that attentuate the open loop gain at nearly 12 db/octave. "Fast rolloff" operational amplifiers require a small feedback capacitor across the feedback resistor in most circuits to provide proper phase margin for stability. For optimum bandwidth, it is suggested that a square wave be applied to the closed loop circuit, and the value of C_f adjusted for the desired transient response at the output. For a range of gains and operational resistances, C_f will vary from one or two pf to perhaps hundreds of pf.

Maximum available closed loop bandwidth is determined by the intersection of the closed loop gain curve (more accurately 1/feedback factor) with the open loop gain curve. The approximate value of C_f may be calculated by selecting a frequency of about 7/10ths of the above intersection frequency as the break frequency (-3db point) of R_fC_f. For R_f less than one megohm, closed loop bandwidth will then be $\omega_{3db} = 1/R_fC_f$.

Maximum closed loop bandwidth of Models 201 and 202, for example, is 5mc at unity gain (the reduction from 10mc is due primarily to the feedback factor of $\beta = 1/2$ for the unity gain inverting configuration). For a closed loop gain of 100, maximum closed loop bandwidth is 800KC. If wide bandwidth is not required, it is suggested that C_f be increased to limit the bandwidth to the minimum value commensurate with system requirement so as to reduce noise.

The Model 203, identical to the Model 202 except for lower frequency response, lower slewing rate, and 6db/octave attenuation, should be considered where wide bandwidth is not required (as in a low frequency integrator), or a high ly reactive load is to be driven.

3.5 Improving Bandwidth & Slewing Rate of Inverting Amplifiers

When circuit design reasons compel large value of feedback resistance for inverting amplifiers, and bandwidth is then limited either by the internal feedback capacitance of approximately 1pf or by an external stabilizing capacitor, C_f, in conjunction with R_f, an improvement in bandwidth may be obtained by shunting R_i with a small capacitor and resistor in series (figure 6).

where $R_iC_i \approx R_fC_f$. R_r should be chosen as perhaps $R_i/10$. A frequency response test or square wave transient response test is suggested for determining optimum values of C_i and R_r.

The published slewing rate specification is determined with

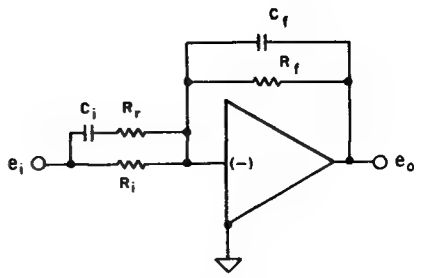


FIGURE 6- IMPROVING BANDWIDTH

small values of input and feedback resistors. Input capacitance of chopper stabilized amplifiers is on the order of one hundred picofarads. This capacitance, or any feedback capacitance, may limit the slewing capability of an amplifier to less than the specification if large values of operational resistors are used. The above technique of adding a small capacitor across the input resistor may also improve slew rate as well as bandwidth.

3.6 Capacitance Loads

Load capacitance, in conjunction with the output impedance of the amplifier can cause oscillations. Figure 7 shows an isolating circuit suitable for most applications with capacitance loads. Connecting the feedback resistance to point A causes less interaction between R (20-100 ohms) and the other circuit values, but results in a higher output impedance (=R). Connecting the feedback resistance to point B achieves extremely small low frequency output impedance since R is inside the feedback loop.

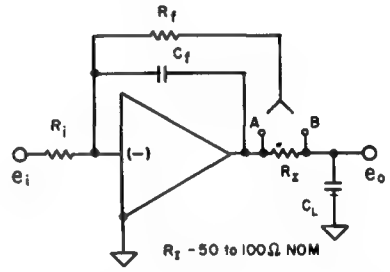


FIGURE 7 - ISOLATING CAPACITANCE LOADS

3.7 Long Leads

All lead connections, including those to the power supply, should be made as short as possible. If it is necessary to have long leads to the feedback network, connect the stabilizing capacitor, C_f, directly from the output terminal to the input terminal.

3.8 Overcoming Large Feedback Resistors

Low level DC amplifier circuits many times require feedback resistors in the 10 to 1000 megohm range. High value, stable, precision resistors are not readily available. The circuit in figure 8 shows one way to circumvent the use of very large resistance values. The gain for this circuit is,

$$\frac{e_o}{e_i} = -\left(\frac{R_1 \| R_f + R_2}{R_1 \| R_f}\right)\left(\frac{R_f}{R_i}\right)$$

which for $R_f >> R_1$ reduces to

$$\frac{e_o}{e_i} = -\left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_f}{R_i}\right)$$

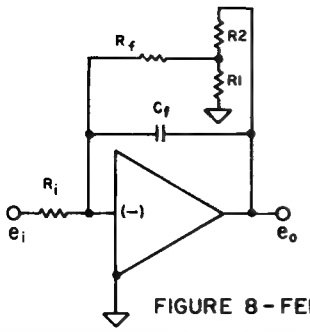


FIGURE 8 - FEEDBACK VOLTAGE DIVIDER

For example, if a closed loop gain of 1000 is required with a summing impedance of 1 megohm, we could select the following circuit values, R_i = 1 megohm, R_1 = 100 ohms, R_2 = 100K ohms and R_f = 1 megohm.

One disadvantage to this technique arises in that voltage drift and noise are increased. Voltage drift referred to the output in the regular configuration for the example above would be

$$\Delta e_o = \left(1 + \frac{1000M}{1M}\right) e_d \Delta T = 1001 e_d \Delta T$$

and for the three resistor network case would be

$$\Delta e_o = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_f + R_i}{R_i}\right) e_d \Delta T$$

$$= \left(\frac{.1K + 100K}{.1K}\right)\left(\frac{1M + 1M}{1M}\right) e_d \Delta T$$

$$= 2002 e_d \Delta T$$

This effect can be minimized by using as small a ratio as practical for $(R_1 + R_2)/R_1$.

3.9 Noise

Noise at the output of an operational amplifier is the sum of various noise components. Input noise voltage is often all that is specified on an amplifier data sheet. This information is sufficient to derive the noise characteristics for a closed loop circuit having gains of 100 to 1000 and very low operational resistances, but additional calculations must be made for other cases. The sources of noise in an operational amplifier circuit are:

1. Input voltage noise of amplifier
2. Input current noise of amplifier
3. Thermal noise of input resistor
4. Thermal noise of feedback resistor
5. Current noise of input resistor
6. Output voltage noise
7. Power supply coupled noise
8. Pick up and RFI

The bandwidth, or frequency characterization of the noise sources, and the degree of correlation between the sources must be also determined for a complete noise analysis.

Broadband noise at the output (exclusive of pick up and RFI) for a circuit with a high closed loop gain and small operational impedances will be approximately the broadband input voltage noise times the closed loop gain. Note that the noise is specified for a particular noise bandwidth (also called a "brick wall" or ideal filter bandwidth). The noise measurement must be made with this filter inserted between the amplifier and the measuring device. If a single pole filter is used in place of the " brick wall " filter, a -3db point of about 63% of the noise bandwidth must be chosen to compensate for the 6db/octave slope of the single pole filter instead of the infinite slope of the ideal filter.

A brief indication of the calculations will be illustrated. The circuit of figure 9 will be used for the analysis.

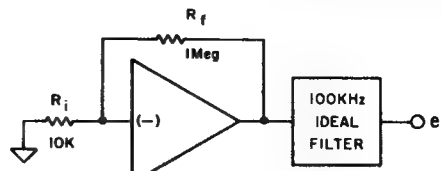


FIGURE 9 - NOISE EXAMPLE

Assume an input voltage noise of 10μV RMS over a noise bandwidth of 100KC. Output noise from this source will be 1 mV RMS. Broadband current noise for the amplifier can be about 1 nA RMS; with 1 megohm feedback resistor, output noise will be 1mV RMS from this source.

Assuming the input voltage and current generators to have a correlation coefficient of 0.3 (a typical value for these amplifiers), the output noise is

$$\sqrt{(1mV)^2 + 2 \times .3 \times 1mV \times 1mV + (1mV)^2}$$

$$= 1.61mV \text{ RMS RTO}$$

Thermal noise of any impedance Z is

$$E_{th(rms)} = \sqrt{4KT\Delta fR}$$

where $\sqrt{4KT} = 1.3 \times 10^{-10}$ at 25°C

Δf is the ideal filter bandwidth over which the noise is measured.
R is the real part of the impedance Z.

Thermal noise of the input resistor (referred to the output) is

$$E_{th(rms)} = 100 \times 1.3 \times 10^{-10} \sqrt{100KC \times 10K\Omega}$$

$$= .4mV \text{ RMS RTO}$$

This will be an uncorrelated noise source and so will add in quadrature to the other noise sources.

We now have $\sqrt{1.61^2 + .4^2} = 1.66mV$ RMS RTO

Thermal noise of R_f is 40μV RMS RTO which will be insignificant in the present example.

Resistor current noise is noise generated in an conventional resistor when current passes through it. The spectral density has a 1/f characteristic with wirewound and some metal film resistors having a coefficient of perhaps .1μV RMS per volt applied per decade of frequency and noisy carbon composition or film resistors having as much as 10μV RMS per volt per decade. The current noise due to a noisy input resistor in the present circuit considered from 1cps to 100KC (5 decades) would be

$$E_{c(rms)} = 100 \times \frac{10\mu V}{V} \times .1V \times \sqrt{5}$$

$$= .22mV \text{ RMS RTO}$$

The .1V is full scale input voltage; current noise is a linear function of input and would obviously contribute no noise with zero input. The noise at full scale would now be 1.68mV RMS RTO.

This particular calculation shows equal effects due to amplifier input voltage and current noise with much reduced effects due to other causes. Other cases may show a much different proportion of effects, for example, resistor current noise would show a marked change in respect to other contributions if a narrower bandwidth were used.

3.10 Multiplexing

When multiplexing (sometimes called scanning or commutating) into a chopper stabilized amplifier with millivolt level signals, certain errors arise that can be minimized by certain precautions. Intermodulation with the chopper drive frequency will show up as signal output errors which are possible to minimize by choosing a scan rate that will not interact with the chopper frequency. Chopper frequency for Models 201, 202, and 203 is about 35Hz and for Model 210 about 150Hz. Harmonics of these frequencies must also be considered when choosing the scan rate.

On special order the Model 201, 202, and 203 may be obtained with provisions for externally driving the chopping oscillator at the scanning frequency or sub-multiples of the scanning frequency. This will eliminate intermodulation noise. The driving frequency must be 35Hz ±1%.

High speed multiplexing, that is, scan rates in the kilocycle region, will cause a shift in the baseline for any chopper stabilized amplifier. This is due to inability of the amplifier output to follow the input switched risetime, generating spikes at the summing junction, and subsequent nonlinear amplification by the chopper amplifier causing base line shift. This problem can be minimized by slowing input rise time, by selecting an amplifier with greater slew rate and full frequency output, or by reducing scan rate.

3.11 Overload Recovery

An internal fast overload recovery circuit is included in these amplifiers to prevent the amplifier output from saturating. Thus the long delays following output saturation which is characteristic of most chopper stabilized amplifiers is avoided.

The internal overload protection circuit is shown below in figure 10. Notice that the fast overload circuit must be externally connected on Models 201, 202, and 203 while it is permanently connected internally on the Model 210.

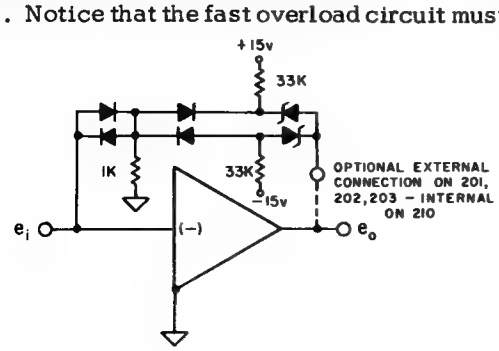


FIGURE 10- INTERNAL OVERLOAD RECOVERY

Rated output voltage for the Model 201, 202, and 203 is ±11 volts without the overload recovery circuit, but it can be as low as ± 9 volts with this circuit connected due to zener tolerances. Minimum output of ± 10 volts with the overload circuit connected can be obtained on special order.

The circuit provides additional feedback current when the amplifier output exceeds the zener plus diode voltage drops. The maximum amount of current that can be fed back is the amplifier's rated output current less the load current, therefore the input overload current must not be allowed to exceed this.

The proper operation of this circuit depends on the following instructions:

1. Power supply voltage must be a minimum of ±15 volts for proper operation.
2. All input overload current must be supplied through the feedback network from the amplifier output in order to maintain linear operation. If the input current plus the load current exceeds the amplifier's rated output current, then the overload recovery circuit will not function properly. For example, a 1000 ohm load resistor draws 10ma. Therfore, with the 202, maximum input overload current cannot exceed 10ma. Input current is normally limited by R_i, but some special circuits (for example, non-inverting amplifiers) may require additional current limiting to retain overload recovery characteristics; refer to paragraph 5.3 for overload protection circuits for non-inverting amplifiers.
3. If the input resistor, R_i, does not adequately limit overload current, an additional stage of silicon diode limiting may be employed as in figure 11 (two diodes in series may be required, R_p can be about 100 to 200Ω).

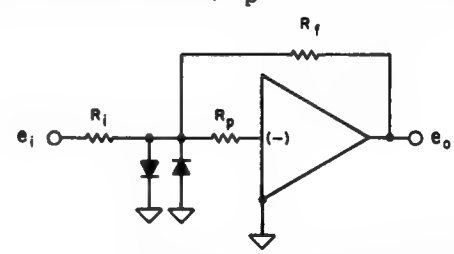


FIGURE 11- OVERLOAD CURRENT LIMITING

Maximum overload transient voltages across the input terminals should be limited to ±50 volts. Due to dissipation limiting, maximum steady state voltage overload to the input should not exceed ±15 VDC.

3.12 Turn On Transient

If the ±15 VDC power supplies do not come on at exactly the same instant, the output of the amplifier will saturate during initial turn on and require as much as thirty seconds to recover on the Models 201, 202, and 203 and about two seconds on the Model 210. This is normal operation for these amplifiers, and, as a matter of fact, for any other chopper stabilized amplifier. Once the amplifier has recovered from the initial turn on transient, it will recover very rapidly from overload due to overdriving the input.

3.13 Power Supply Voltage

Rated specifications depend on the supply voltages being

in the range from ± 15 to 16 VDC. As the supply voltage drops below ±15VDC the overload circuit will not function properly and below 13 to 14 volts the amplifiers operating specifications are degraded.

Model 205 is available for operation from ±12 volt power supplies; specifications are similar to the 202 with reduced output swing. Models are available on special order to operate at other supply voltages.

The amplifiers are relatively insensitive to gradual power supply changes or low frequency variations. However, there is sensitivity to supply voltage AC ripple and transients. For best operation, ripple voltage should be no more than a few millivolts and voltage transients should be decoupled as much as possible.

Low power supply output impedance at high frequencies may be lost through long lead lengths, and local decoupling of the power leads may be required. All models have capacitors connected internally across the power supply terminals to give some local decoupling.

3.14 Accessories

A plug in socket, Model AC 1002, (figure 12) is available which can be used for mounting the amplifier or for aiding in evaluation. A noise shield, Model AC1106 (figure 13),

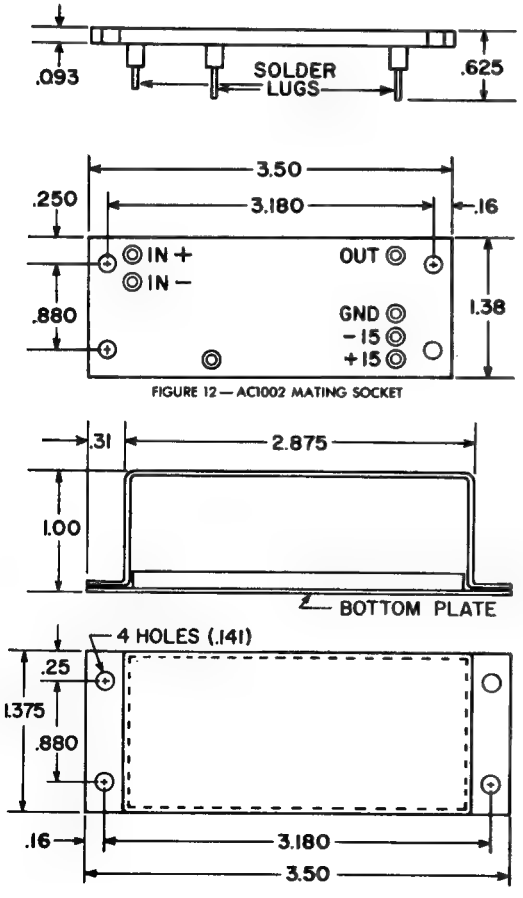


FIGURE 12 — AC1002 MATING SOCKET

FIGURE 13 — AC1106 NOISE SHIELD & HOLD DOWN BRACKET

is also available for reducing the effects of noise pick up in areas of high noise and RFI generation. The AC1106 also serves as a hold down bracket in high shock or vibration environments.

A circuit simulator, Model AC 1100 is available to aid in conveniently breadboarding and evaluating various closed loop circuits. The Model AC1100 is made up of a universal plug in socket and a versatile arrangement of 3/4 inch spaced banana jacks for connecting input, output, and power supply voltages and for plug in of feedback components mounted on banana plugs.

4.0 DEFINITION AND MEASUREMENT OF INPUT OFFSET DRIFT

4.1 Offset Drift Sources

An equivalent circuit for offset drift is shown in figure 14.

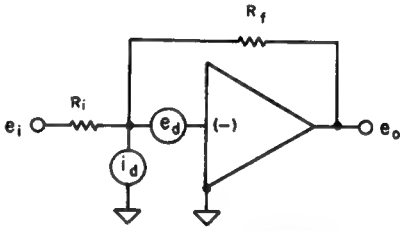


FIGURE 14 - EQUIVALENT INPUT DRIFT GEN.

The drift generators e_d and i_d include the effects of temperature changes, supply voltage changes, time, and internal gradients due to self-heating. Voltage source drift referred to the output is given by

$$\Delta e_o = e_d \left(1 + \frac{R_f}{R_i}\right)$$

and current source drift by

$$\Delta e_o = i_d R_f$$

e_d is determined by calculating the sum of three components; the expected variation in ambient temperature in degrees C times the temperature coefficient of voltage drift in μV/°C, the change in supply voltage in % times the coefficient of voltage drift per % change in supply, and the drift of voltage offset with time.

i_d is determined in a similar way. Total worst case output drift due to the above six drift coefficients is

$$\Delta e_o = e_d \left(1 + \frac{R_f}{R_i}\right) + i_d R_f$$

which, if referred to the input, becomes

$$\Delta e_i = e_d \left(1 + \frac{R_i}{R_f}\right) + i_d R_i$$

where e_d and i_d are implied to each be the sum of three components.

In addition to the above sources of drift within the amplifier, the drift characteristics of the external voltage and current offset adjustment networks must be investigated for extremely critical applications. The change in value of the potentiometers and resistors with time and temperature must be calculated and added to the previous drift calculation.

For an additional analysis of drift sources, refer to "Operational Amplifiers - Part IV" published by Analog Devices.

4.2 Voltage and Current Drift Measurements

The measurement of extremely low levels of voltage and current drift impose a severe problem on instrumentation. A method suitable for amplifying input voltage offsets to levels which can be easily measured or recorded is shown in figure 15. The low value of input resistor reduces the effect of input current drift to a value negligible in relation to the voltage drift. Sensitivity of the circuit is 1mV output per microvolt of drift e_d.

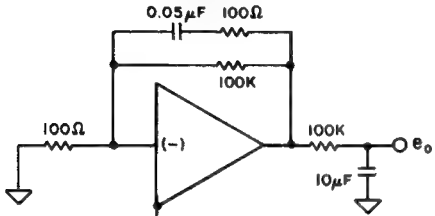


FIGURE 15 - VOLTAGE DRIFT

Figure 16 shows a circuit for measuring input current offset. The 10 megohm resistor produces a voltage due to current offset which is much larger than the effect of voltage offset of the amplifier. Sensitivity of the circuit is 1mV output per picoamp of drift, i_d.

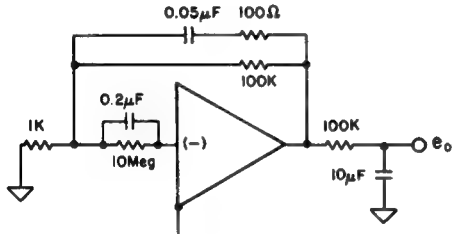


FIGURE 16 - CURRENT DRIFT

5.0 APPLICATIONS AND CIRCUITS

5.1 Inverting Amplifier

The conventional inverting amplifier is illustrated in figure 17. Scaling is accomplished by varying ratio R_f/R_i.

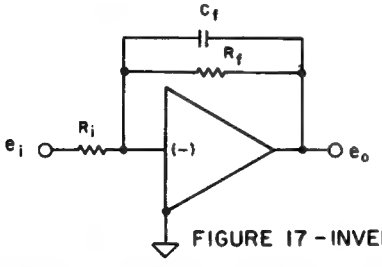


FIGURE 17 - INVERTING AMPLIFIER

Gain of greater or less than unity is practical with typical range from .1 to 5,000. Widest bandwidth and fastest slew rate is obtained when using smallest practical resistor values. See paragraph 3.4 for determining value of C_f. Note that output must drive R_f as well as external load, therefore, output current available for load is reduced by E_{fs}/R_f.

Input impedance equals R_i; output impedance is usually a fraction of an ohm at DC, rising to values around 100 ohms at high frequencies.

5.2 Summing Amplifier

The summing amplifier may be used for scaling at the same time.

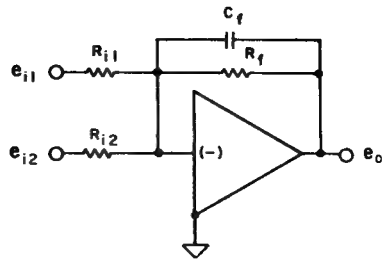


FIGURE 18 - SUMMING AMPLIFIER

$$e_o = -\left(\frac{R_f}{R_{i1}}\right) e_{i1} - \left(\frac{R_f}{R_{i2}}\right) e_{i2}$$

Bandwidth of a multiple input summing amplifier is less than a single input inverting amplifier even though all impedances may be equal, because of the reduction in feedback factor (β). Feedback factor is the attenuation ratio of the operational impedances, which for a two input summing amplifier is

$$\beta = \frac{R_{i1} \| R_{i2} \| R_{IN}}{R_{i1} \| R_{i2} \| R_{IN} + R_f}$$

Output noise voltage and drift are increased over inverter values also for the same reason. In the drift case,

$$e_d \left(1 + \frac{R_f}{R_{i1} \| R_{i2}}\right)$$

is the expression for output drift of a two input summing amplifier which may be compared with $e_d(1+R_f/R_i)$ for an inverter.

5.3 Non-Inverting Amplifiers (High Input Impedance)

The single ended input (inverting only) of chopper stabilized amplifiers make special circuitry a requisite for obtaining a non - inverting output from a single amplifier. The general condition is input, output, and power supply grounds cannot all be common. Stated another way: either the input, the output, or the power supply must be floating (isolated) with respect to the remaining two circuit grounds (which two may usually be common).

When an isolated or floating power supply is required, the foremost consideration is the degree of isolation between input power and output power. Resistance values of 1000 megohms and an effective capacitance range of .01 to .1pf are possible in a well built, double shielded transformer, and the floating power supply should have specifications of this magnitude. Some applications may not require the degree of isolation of others, however, the unguarded or effective capacitance and leakage resistance should be known before attempting to use a power supply in a floating configuration.

Voltage Follower (Power Supply Floating)

Here, the regular output of the amplifier is grounded and used for the input and output returns. The output is taken from the floating power supply common terminal. Input impedance is typically 1000 megohms at DC (depending on the isolation of the floating power supply). Bandwidth is full amplifier small signal bandwidth. Offset current compensation if required is in conventional manner (see figure 5) except that 50 K pot is connected across floating power supplies.

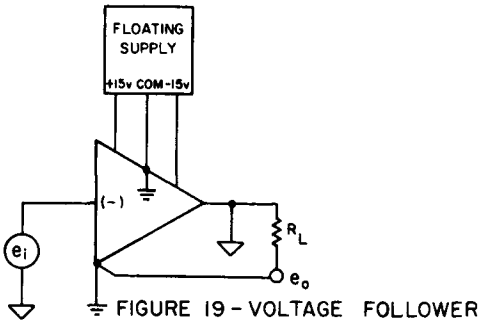


FIGURE 19 - VOLTAGE FOLLOWER

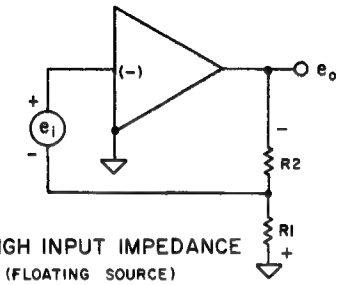


FIGURE 20 - HIGH INPUT IMPEDANCE
(FLOATING SOURCE)

Gain of the circuit in figure 20 is $(R_1 + R_2) / R_1$.

Source must be truly floating or improper operation will result. Input impedance is >100 megohms at DC typically. (Actually, for low source impedance, input impedance at DC = $R_{in} \times A\beta$ where A is the DC gain, β is $R_1/(R_1+R_2)$ and R_{in} is the amplifier open loop input resistance).

Offset current may be compensated in the usual manner by injecting current into the amplifier input.

Gain (at DC) is limited to greater than or equal to unity. For gains of less than unity, the inverting connection must be used, or an input voltage divider is required.

Grounded Source (Floating Output and Power Supply)
If a grounded source must be amplified, and the output load and power supply can be floated, the same circuit as the preceeding may be used giving the advantages of high input resistance and high speed.

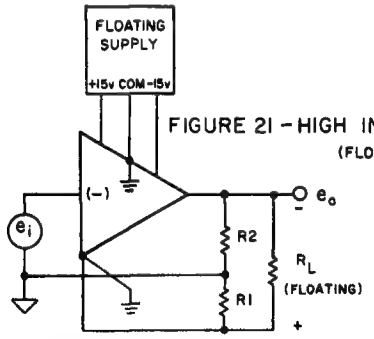


FIGURE 21 - HIGH INPUT IMPEDANCE
(FLOATING LOAD)

Two Amplifier High Input Impedance Circuits

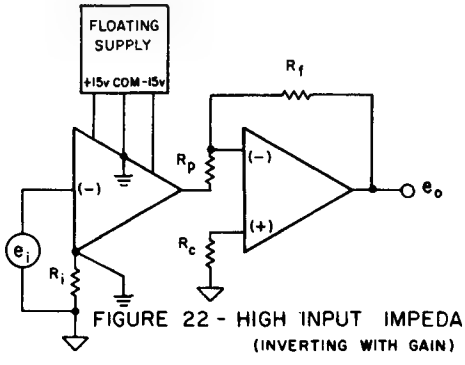


FIGURE 22 - HIGH INPUT IMPEDANCE
(INVERTING WITH GAIN)

Characteristics of the circuit of figure 22 are high input impedance, wide bandwidth, and high gain if desired together with a grounded load. Gain is the ratio of R_f/R_i, R_p is a small value for overload current limiting and R_c is the usual parallel equivalent of R_p and R_f for offset drift compensation.

The input voltage, e_i, appears across R_i producing a current e_i/R_i which must flow out of the amplifier output, since the power supply is floating. This current flows into the summing junction of the output amplifier and appears across R_f, thus the gain is

$$e_o = \frac{e_i}{R_i} \times R_f = e_i \times \frac{R_f}{R_i}$$

Models 106 and 108 will be satisfactory for the output amplifier in most applications since drift of the output is divided by R_f/R_i referred to the input, e_i. It is important to keep resistor values very low; preferably R_f should be 2K or lower although output current limitations set a limit on the size.

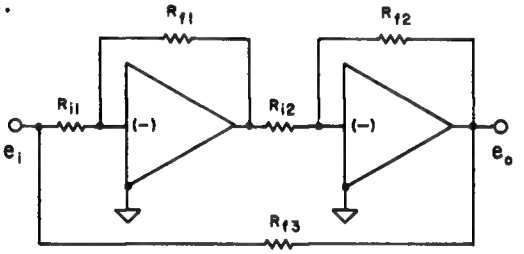


FIGURE 23 - HIGH INPUT IMPEDANCE
(BOOTSTRAPPED INPUT - GROUNDED SUPPLY)

The circuit of figure 23 provides a high input impedance because of the positive feedback to the input through R_{f3}. Gain may be equally divided between the two amplifiers or may be taken mostly in the first amplifier therefore reducing the drift requirements of the second amplifier, in this case R_{f3} is chosen $\geq (R_{f1} \times R_{f2})/R_{i2}$.

Maximum input impedance occurs when R_{f3} is exactly equal to $(R_{f1} \times R_{i2})/R_{i2}$. Source impedance must be small with respect to R_{f3} to prevent oscillations from occurring.

Overload Current Limiting

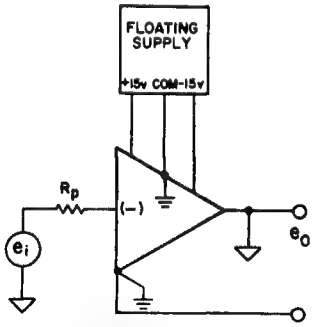


FIGURE 24 - OVERLOAD CURRENT LIMITING

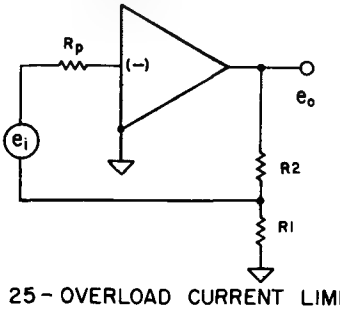


FIGURE 25 - OVERLOAD CURRENT LIMITING
(FLOATING SOURCE)

The voltage follower and non-inverting configurations require a current limiting resistor at the input (figures 24 and 25) for proper operation of the high speed overload circuit.

R_p should be the smallest value possible commensurate with anticipated overload to avoid additional phase shifts . Again, the extra diode limiter may be of value (figure 26) .

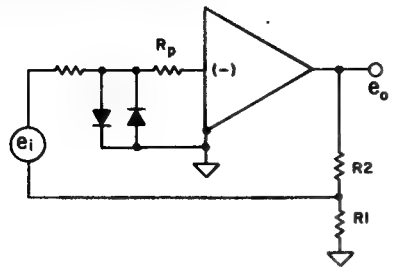


FIGURE 26 - ADDITIONAL CURRENT LIMITING
(DIODE LIMITER)

5.4 Differential Input Configuration

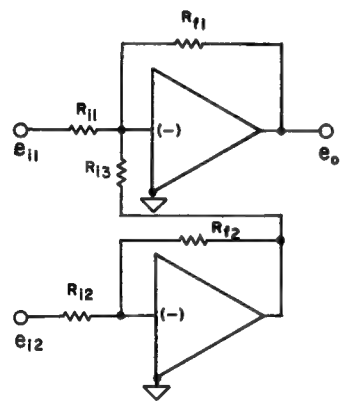


FIGURE 27- DIFFERENTIAL INPUTS

Figure 27 shows an obvious method of forming a differential connection, and is probably the simplest and easiest to use. An extension of the voltage follower is shown in figure 28. The circuit is suitable for gains of unity to 50 or so, but higher gains become noisy, since the input noise of all three amplifiers is additive (at quadrature for uncorrelated noise sources).

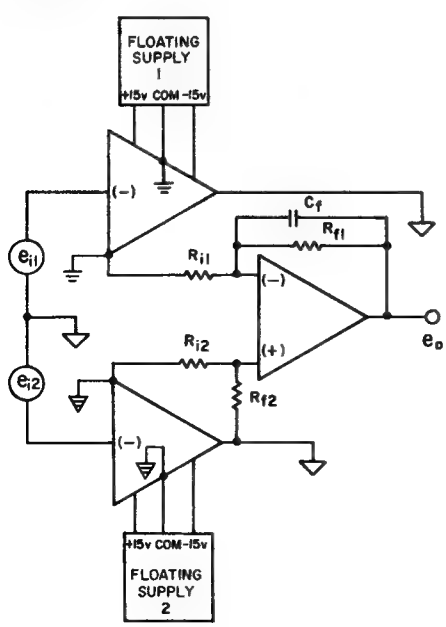


FIGURE 28 - HIGH INPUT IMPEDANCE DIFFERENTIAL INPUT

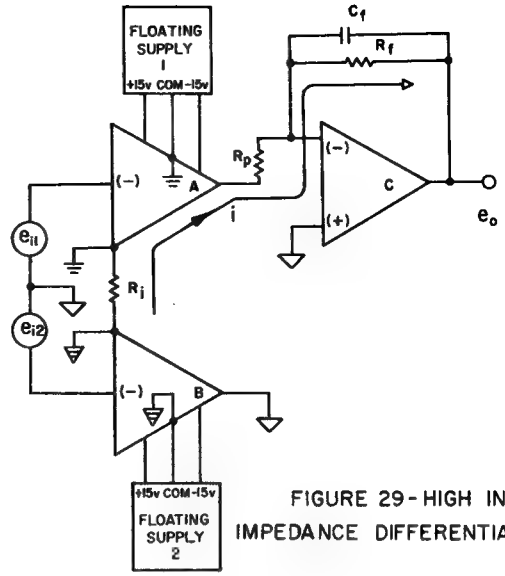


FIGURE 29 - HIGH INPUT IMPEDANCE DIFFERENTIAL INPUT

The circuit of figure 29 is suitable for gains of unity to several thousand. Operation is as follows: the voltage $e_{i1} - e_{i2}$ appears across R_i (as if the two input amplifiers were voltage followers), the current $(e_{i1} - e_{i2})/R_i$ flows out of A's output into the summing junction of C and through R_f (R_p is only for overload protection). Therefore gain is R_f/R_i. Input impedance is hundreds of megohms, being limited usually by the isolation of the floating power supplies. Amplifier C can be any non-stabilized differential amplifier with suitable bandwidth and stability characteristics (Model 203 for A and B and Model 108 for C are suggested for low noise, moderate bandwidth).

With Models 202 or 210, bandwidths of hundreds of kilocycles may be obtained with extremely high input resistance at DC. For the overload protection to be operative, small resistors must be incorporated in series with each input. Care must be exercised in stabilization of this circuit due to the extremely large forward gain of the total configuration.

5.5 Integrating Amplifier

The exceptional voltage and current drift specifications, together with high open loop gain make the 200 Series amplifiers particularly well suited for use as integrators. Model 203 is designed especially for integrating applications and is recommended in all cases except where the bandwidth of Models 202 or 210 is required or possibly where the lower cost and more modest performance of the Model 210 is acceptable.

The specifications of importance for an integrator are voltage offset and drift, current offset and drift, open loop gain, and input resistance. Drift rate of the integrator is obviously related to voltage and current drifts; additional droop of a held value (and non-linearity during integration) results from the finite values of input resistance and DC gain. The measure of droop (in addition to offset contributions) is calculated by assuming a resistor in parallel with the integrating capacitor equal to $R_{IN} \times$ DC gain and computing the discharge rate.

The main causes of integrator error are voltage and current offsets and change of offset. Initial offset can be adjusted to zero, but drift (change of initial offset) with time, temperature, and supply voltage, cannot be compensated for and must be specified sufficiently low to maintain system accuracy. Voltage offset and current offset at any parti-

cular temperature can be compensated for at the same time with either a voltage offset trim or current offset trim as long as R_i is constant. If R_i must change in value (be switched in value for example) or if integration is stopped by open circuiting the source ($R_i \to \infty$) instead of grounding the input, then voltage and current offsets must be adjusted independently with separate trim pots for most accurate results.

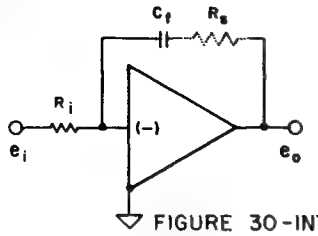


FIGURE 30 - INTEGRATING AMPLIFIER

The conventional circuit is shown in figure 30. For a constant held input voltage, output rate of change is $1/R_iC_f$ volts/second per volt of input signal.

Voltage drift rate due to voltage offset is

$$\frac{\Delta e_o}{\Delta t} = \frac{e_d}{R_iC_f}$$ and for current offset is

$$\frac{\Delta e_o}{\Delta t} = \frac{i_d}{C}$$, where e_d and i_d are defined in 4.1.

To minimize total drift for any given time constant, R_iC_i observe that voltage drift is dependent only on the product R_iC_f, and cannot be minimized except by increasing the time constant or choosing a better amplifier. However, current drift can be minimized by choosing C as large as possible.

A small resistor, R_s, in series with C_f, may be required for proper stabilization with wide bandwidth amplifiers.

5.6 Photomultiplier Tube Amplification And Current To Voltage Converters

Photocells, photomultipliers, ionization chambers and a host of other scientific instruments have extremely high effective source impedances and low output currents. Devices of this nature approach an ideal current generator in performance and can be treated as such for choosing circuit approaches.

An instrumentation method usual in the past has been to insert a large value resistor in series with the output of the current source, and measure the voltage drop across this resistor with an amplifier having very high input impedance and very low offset current.

A circuit configuration that in many instances will provide superior results is shown in figure 31.

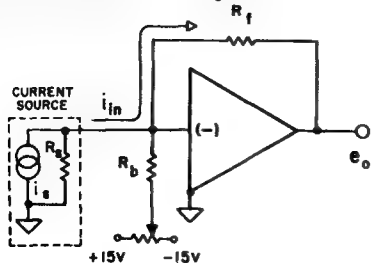


FIGURE 31 - CURRENT to VOLTAGE CIRCUIT
(PHOTOMULTIPLIER act.)

This is the familiar inverting amplifier used for current to voltage conversion. A current i_{in} is produced by the source, (and neglecting for the moment R_b) almost all of i_{in} will flow through the feedback resistor, R_f, since the input current to actuate the amplifier is extremely small. The output voltage will then be $i_{in} \times R_f$. The transfer function for the circuit is in the form of a transimpedance, $e_o/i_{in} = R_f$. The function of R_b is to offset any initial current from the source, for example, dark current in a photomultiplier tube, and to compensate for the small offset current of the amplifier. Notice that R_b does not load the current source, for the input to the amplifier is a current summing junction and therefore a virtual ground.

Advantages of this arrangement compared to a high input impedance voltage follower amplifying the signal produced across a load resistor are as follows:

1. Linearity of most transducers is improved; current sources show maximum linearity working into a voltage node. If linearity errors arising from large values of load resistance are attempted to be improved by reducing the load resistor and increasing voltage gain of the amplifier, then voltage drift and voltage noise are increased by the amount of the voltage gain.
2. Common mode voltage errors of a voltage follower circuit are eliminated.
3. Initial offset currents much larger than the dynamic range of the signal input are easily zeroed by choosing a value of $R_b < R_f$.
4. Input impedance changing with time and temperature can produce appreciable error in the voltage follower.

Noise and drift at the output will be due primarily to current noise and drift. Input voltage noise and drift are not amplified in a transimpedance and in a practical case, the output contribution due to the equivalent input voltage noise and drift generators will be at most twice the input values.

Output current noise and drift are as usual $i_n R_f$ and $i_d R_f$ respectively. For best signal to noise characteristics, a feedback capacitor should be included to limit the bandwidth to that required for system performance.

5.7 Precision Voltage Source

A precision variable (or fixed) voltage reference source is illustrated by figure 32.

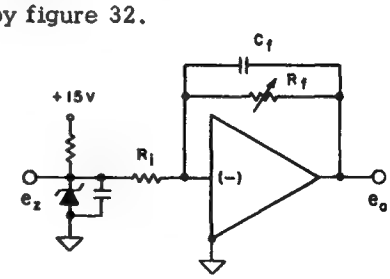


FIGURE 32 - PRECISION VOLTAGE SOURCE

This arrangement provides a linear relation between R_f and output voltage so that a calibrated variable resistance will produce a calibrated output voltage. A temperature compensated zener reference can be used for precision stability or a conventional 5.6 volt zener for moderate stability requirements. Various switching schemes can be devised to obtain bi - polar outputs. R_i is usually between a few thousand ohms and a hundred thousand ohms. C_f should

be a low leakage capacitor as large as practical. Model 203 is recommended for this application. See paragraph 3.6 if large capacitive loads must be driven.

5.8 Current Sources

For current source applications it should be noted that the Model 201 has a hefty 100ma output rating while the Models 202, 203, and 210 all produce 20ma.

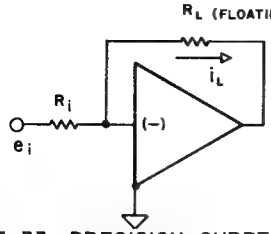


FIGURE 33 - PRECISION CURRENT SOURCE

Figure 33 shows a precision current source with a requirement that the load must be floating.

Current through R_L is e_i/R_i, Limitations on size of R_L are maximum voltage drop across R_L and maximum current through R_L to be within amplifier output specifications.

By using a floating power supply, a precision current source may be constructed as in figure 34.

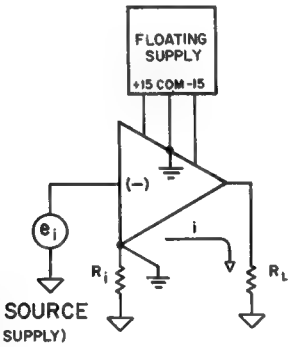


FIGURE 34 - CURRENT SOURCE (FLOATING SUPPLY)

The input voltage, e_i, appears across R_i, producing the current i. Because of the floating power supply this current in turn must flow through R_L for a return path. Note that if e_i is about 10 volts, the output can swing from 0 to +20 volts, giving a greater range than other techniques.

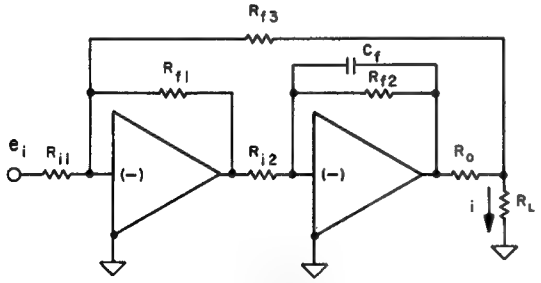


FIGURE 35 - CURRENT SOURCE (GROUNDED SUPPLY)

The circuit of figure 35 produces a current of

$$\frac{R_{f3} \times E_1}{R_{i1} \times R_o}$$

through R_L with the requirement that $R_{f3} >> R_L$.

Precisely this current flows through R_o, but a small amount must be channeled through R_{f3}, therefore the current in R_L is low by the amount in R_{f3}.

If Models 201, 202, or 210 are used, feedback capacitors will be required as usual. With Model 203, a feedback capacitor on the second amplifier will reduce noise and provide additional stability for the circuit. Suggested values are $R_{i1} = R_{f1} = R_{i2} = R_{f2} = R_{f3} = 100K$ and $R_o = 100\ \Omega$ for 10ma output per volt input or $R_o = 1K$ for 1ma output per volt input.

5.9 Bridge Amplifier (Floating Bridge Supply)

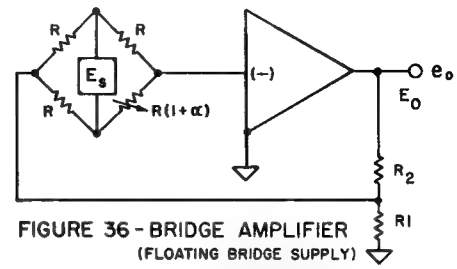


FIGURE 36 - BRIDGE AMPLIFIER (FLOATING BRIDGE SUPPLY)

Figure 36 illustrates the use of a non-inverting high input impedance configuration for amplifying a low level bridge signal. Output for a single active arm is

$$e_o = \left(\frac{R_1 + R_2}{R_1}\right) \left(\frac{E_s}{2(2+\alpha)}\right)$$

ANALOG
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AN OPERATIONAL AMPLIFIER APPLICATION MANUAL

OPERATIONAL AMPLIFIERS

PART I – Principles of operation and analysis of errors.

PART II – Inverting, non-inverting and differential configurations.

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OPERATIONAL AMPLIFIERS, PART I
Principles of operation and analysis of errors

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The term "operational amplifier" was orginally coined by those in the analog computer field to denote an amplifier circuit which performed various mathematical operations such as integration, differentiation, summation and subtraction. Although operational amplifiers are still widely used for analog computation, the application of these devices has been so vastly extended that the terminology is now archaic. Today, the widest use of operational amplifiers is in such applications as signal conditioning, servo and process controls, analog instrumentation and system design, impedance transformation, voltage and current regulators and a host of other routine functions.

Non-linear applications of operational amplifiers have also been added to the growing frontier of analog amplifier technology. In this category, operational amplifiers are used for voltage comparators, A to D and D to A converters, logarithmic amplifiers, non-linear function generators and ultra-linear rectifiers, to name only a few applications.

An operational amplifier is generally characterized by the following properties:

- Extremely high dc voltage gain, generally in the range from 10^4 to 10^9.
- Wide bandwidth starting at dc and rolling off to unity gain at from 1 to 100 Mc/s with a slope of 6 db/octave or at most 12 db/octave.
- Plus and minus output voltage over a large dynamic range, generally from ± 10 to ± 100 v.
- Very low input dc offset and drift with time and temperature.
- High input impedance so that amplifier input current can be largely neglected.

The great versatility and many advantages of operational amplifiers stems from the use of negative feedback. You recall from circuit theory that negative feedback tends to improve gain stability, to reduce output impedance, to improve linearity and in some configurations, to increase input impedance. As shall be pointed out later, the extent to which closed loop performance is improved by negative feedback, depends on the magnitude of loop again ($A\beta$).

Another useful property of negative feedback, which is the basis for all operational amplifier technology, is that with enough gain, the closed loop amplifier characteristics become a function of only the feedback components. For example, the gain of the closed loop circuit in Fig 1 is determined almost entirely by the ratio of the two resistors, Z_f/Z_i and is largely independent of the open loop characteristics of the operational amplifier. Since the selection and configuration of the feedback components determine the operation of the circuit, the versatility in applying operational amplifiers is limited primarily by your ingenuity in selecting and configuring the feedback components.

OPERATIONAL AMPLIFIER CHARACTERISTICS

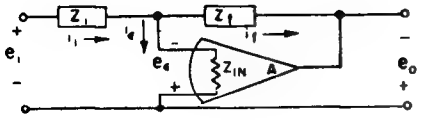
An ideal operational amplifier would have infinite open loop gain and bandwidth and zero input noise, offset and drift. In this case the feedback components determine entirely the closed loop performance and the operational amplifier has absolutely no effect on the circuit performance. Although, of course, no amplifier has these ideal qualities, the performance of modern solid state amplifiers closely approaches these limits. To discuss the limitations of practical amplifiers and how these limitations effect closed loop performance, the errors due to the non-ideal characteristics of operational amplifiers are classified into four basic categories:

- Static errors due to finite amplifier gain.
- Dynamic errors due to bandwidth limitations.
- Errors due to initial voltage and current offsets and drift caused by temperature change, time stability and supply voltage change.
- Errors due to noise.

There are also more refined considerations such as common mode voltage characteristics and finite input and output impedances which effect the performance of operational amplifier circuits.

Static Errors Due to Finite Amplifier Gain

The most distinguishing feature of operational amplifiers is the staggering magnitude of dc voltage gain which they boast. Even the least expensive differential amplifiers have voltage gains of 10^4 while high performance chopper stabilized units have gains as high as 10^9. Negative feedback around this high voltage gain, accomplishes the virtues of closed loop performance and



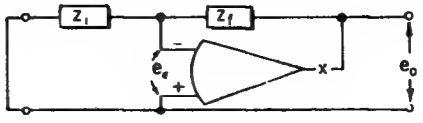


Fig 1 (Left) — Operational amplifier circuit. Fig 2 (Right) — Circuit to determine the feedback attenuation β.

makes the circuit dependent only on the feedback components.

Before proceeding to a mathematical analysis of operational circuit performance, it is interesting to intuitively examine the significance of voltage gain. Suppose, as an extreme case, you assume that the amplifier in Fig 1 has a dc voltage gain of 10^8 and a maximum output voltage ± 10 v dc. In all other regards, suppose that the amplifier is ideal which among other things implies that $e_o = o$ when $e_i = o$. You can then state that when the output voltage swings through its extremes of $+10$ to -10 v dc, the error voltage, e_ϵ, will not vary by more than ± 0.1 μv from ground. The currents through Z_i and Z_f are then:

$$i_i = (e_i - e_\epsilon)/Z_i \approx e_i/Z_i \qquad (1)$$

$$i_f = (e_\epsilon - e_o)/Z_f \approx -e_o/Z_f \qquad (2)$$

To go further, let us say that in this circuit the ratio of Z_f/Z_i is selected so that the output voltage will be $+10$ v dc when the input is -10 mv which states that the closed loop gain, e_o/e_i, is 1000. Since the error voltage will not exceed 0.1 μv, e_ϵ is completely negligible compared to e_o and an error of less than 0.001% (0.1 μv/10 mv), is committed by neglecting e_ϵ as compared to e_i. Assuming that $e_\epsilon = o$, implies that $i_\epsilon = 0$, which, for any practical value of Z_{IN}, is an excellent assumption. If $i_\epsilon = o$, then,

$$i_i = i_f \qquad (3)$$

From Eqs (1) and (2), the closed loop gain, determined entirely by the ratio of Z_f and Z_i, is:

$$e_o/e_i = -Z_f/Z_i \qquad (4)$$

This simple example shows the validity of two basic assumptions which underlie the analysis of all operational amplifier circuits, namely:

- Feedback current, i_f, is equal to the input current, i_i, since error current, i_ϵ, is negligible.
- The error voltage, e_ϵ, across the operational amplifier input terminals is assumed to be zero volts.

To repeat, these assumptions follow from the fact that negative feedback, coupled with high open loop gain, constrains the error voltage and consequently the error current to infinitesimal values. The higher the gain, the more valid these assumptions become.

Quantitative Gain Error Analysis: To develop quantitative expressions for the errors caused by finite amplifier gain, assume that the amplifier in Fig 1 is ideal except for finite gain. These assumptions can be stated quantitatively as:

$$Z_{IN} = \infty,\ e_o = o \text{ when } e_i = o$$

$$Z_{out} = o,\ \omega_o = \infty \ (\textit{infinite bandwidth})$$

For an amplifier with open loop voltage, A, the exact closed loop gain is,

$$\frac{e_o}{e_i} = -\underbrace{\left[\frac{Z_f}{Z_i}\right]}_{\substack{\textit{ideal}\\ \textit{amplifier}}} \underbrace{\left[\frac{1}{1+(1/A)(1+Z_f/Z_i)}\right]}_{\substack{\textit{error factor due}\\ \textit{to finite voltage gain}}} \qquad (5)$$

As the gain, A, approaches infinity, eq (5) reduces to the form of an ideal operational circuit:

$$e_o/e_i = -Z_f/Z_i \qquad (6)$$

Consequently, the error in closed loop gain, e_o/e_i, due to finite open loop gain, A, is:

$$\textit{error factor} = \frac{1}{1+(1/A)(1+Z_f/Z_i)} \qquad (7)$$

If we let $1/\beta = 1 + Z_f/Z_i$ eq (7) can be rewritten

$$\textit{error factor} = \frac{1}{1+1/A\beta} \approx 1 - 1/A\beta, \textit{ for } A\beta >> 1$$

The error factor is in a form which, when multiplied by the ideal closed gain, gives the actual closed loop gain. The percentage error due to finite gain A is:

$$\varepsilon(\%) = 100/A\beta \qquad (8)$$

Gain Stability: Closed loop gain error, eq (8), is not in itself tremendously important since the ratio Z_f/Z_i can always be adjusted to compensate for this error. However, closed loop gain stability is an important consideration in most applications. Closed loop gain stability is effected primarily by variations in open loop gain due to changes in temperature and load or due to aging of amplifier components. Redefining closed loop gain by $G_{cl} = e_o/e_i$, then

$$\frac{\Delta G_{cl}}{G_{cl}} \approx \frac{\Delta A}{A} \quad \frac{1}{A\beta} \qquad (9)$$

From eq (9) any variation in open loop gain, A, is reduced by the factor Aβ in its effect on closed loop gain, G_{cl}. Improvement in gain stability is one of the important benefits of negative feedback.

Loop Gain

The product Aβ which occurs in eqs (8) and (9), is called loop gain, a well known term in feedback theory. The improvement in closed loop performance due to negative feedback is, in nearly every case, proportional to loop gain.

To a first approximation, closed loop output impedance, linearity and gain stability, are all reduced by Aβ with negative feedback. Term β, generally called feedback attenuation, is defined as the factor by which the output voltage, e_o, is attenuated to produce the error voltage, e_ϵ, with the forward gain open and with the input source replaced by its Thevin equivalent resistance. Assuming zero source resistance, by definition $1/\beta$ from the circuit in Fig 2 is:

$$\frac{\Delta e_o}{\Delta e_\epsilon} = \frac{Z_i + Z_f}{Z_i} = 1 + \frac{Z_f}{Z_i} = \frac{1}{\beta} \qquad (10)$$

For $Z_f > Z_i$, which is generally the case for closed loop gain greater than one:

$$1/\beta \approx Z_f/Z_i = e_o/e_i = G_{cl} \qquad (11)$$

Consequently, loop gain, Aβ, is approximately the ratio of open loop gain to closed loop gain,

$$A\beta \approx A/G_{cl}$$

This discussion emphasizes that the loop gain is the significant factor in predicting the performance of closed loop operational amplifier circuits. The open loop gain required to obtain an adequate amount of loop gain will, of course, depend on the desired closed loop gain. For example, an amplifier with an open loop gain of 20,000 will have a loop gain of 2000 for a closed loop gain of 10, but only a loop gain of 20 for a closed loop gain of 1000.

Frequency Dependence of Loop Gain: Thus far, it was assumed that the open loop gain is independent of fre-

quency. Unfortunately, this is not the case. Leaving the discussion of the effect of open loop response on bandwidth and dynamic errors until later, let us now investigate the effect of frequency response on loop gain and static errors.

The open loop frequency response for a typical operational amplifier with superimposed closed loop amplifier response for a gain of 100 or 40 db, illustrates graphically (Fig 3) these results:

- Loop gain in db is the difference between open loop gain and closed loop gain. Actually loop gain is the ratio between open and closed loop gain, but subtracting on a logarithmic scale is equivalent to normal division.
- Loop gain decreases with increasing frequency due to the attenuation of open loop gain.
- Loop gain decreases for higher values of closed loop gain.
- Closed loop gain depends entirely on the ratio of the feedback components, Z_f and Z_i, and is independent of open loop gain (apart from errors which are inversely proportional to loop gain).
- Where the closed loop and open loop curves intersect, loop gain is zero which implies that beyond this point, there is no negative feedback. Consequently, closed loop gain will be equal to open loop gain.

Fig 3 points out that the high open loop gain quoted for operational amplifiers is somewhat misleading. Beyond a few c/s, open loop gain is attenuated rapidly. Consequently, closed loop gain stability, output impedance, linearity and other parameters which depend on loop gain, are degraded at higher frequencies. One of the reasons for having dc gain as high as 10^5 and bandwidth as wide as several Mc/s, is to obtain adequate loop gain at frequencies even as low as 100 c/s.

One approach to improving loop gain at high frequencies other than by increasing open loop gain is to increase open loop bandwidth. Fig 4 illustrates the improvement in loop gain obtained by increased bandwidth. Another approach to improving loop gain at higher frequencies, is to have faster attenuation of the open loop response. Normally, operational amplifiers have 6 db/octave attenuation to provide stable operation for all values of resistive feedback. While it is true that fast roll-off amplifiers are more difficult to stabilize, once the techniques for applying amplifiers with these characteristics are understood, it is just as easy to use them and the high frequency performance is considerably improved over conventional 6 db/octave amplifiers. Fig 5 illustrates the improvement obtained in loop gain at high frequencies by using a fast roll-off amplifier.

Generalized Operational Circuit With Multiple Inputs

In the foregoing analysis the impedances Z_i and Z_f have been used to denote that the feedback elements may be any linear, passive, bilateral networks. These impedances may be complex. For purposes of amplification or isolation, the feedback elements would be resistors, but in other applications such as servo controls, the feedback elements may be rather complicated networks. The same analyses are applicable to non-linear feedback elements such as diodes or transistors.

In the most general cases, it is possible to sum or otherwise manipulate a number of input voltages as shown in Fig 6. In this configuration, the inputs are almost completely isolated from each other due to the very low error voltage at the summing junction.

The generalized closed loop gain equation for this circuit is:

$$e_o = (\textit{ideal amplifier})\ (\textit{error factor due to finite gain}) \tag{12}$$

where:

$$(\textit{ideal amplifier}) = e_1 \frac{Z_f}{Z_1} + e_2 \frac{Z_f}{Z_2} + \ldots + e_N \frac{Z_f}{Z_N}$$

and $(\textit{error factor}) =$

$$\frac{1}{1 + (1/A)\left(1 + \frac{Z_f}{Z_1} + \frac{Z_f}{Z_2} + \ldots + \frac{Z_f}{Z_N}\right)}$$

$$\textit{or } e_o = -\left[\sum e_i \frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + (1/A)(1 + Z_f/Z_p)}\right]$$

where Z_p is the parallel sum of $Z_1, Z_2 \ldots Z_N$.
For any one input voltage eq (12) reduces to the form of eq (6),

$$\frac{e_o}{e_i} = -\left[\frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + \frac{1}{A\beta_p}}\right]$$

Except now,

$$1/\beta_p = 1 + \frac{Z_f}{Z_p}$$

All of the preceding discussions and results are equally applicable to the circuit in Fig 6, except that loop gain, $A\beta_p$, for this case may be considerably reduced due to the parallel sum of the input impedances. The errors due to finite loop gain will be increased by the ratio β/β_p. Since the loop gain for all inputs is the same, if any one input impedance is low, the ensuing errors for all other inputs are also increased.

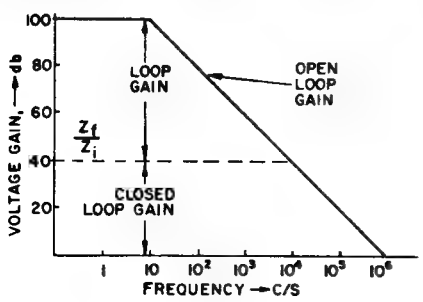


Fig 3 — Open loop frequency response.

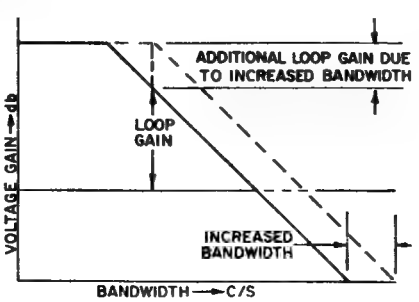


Fig 4 — Effect of increased bandwidth on loop gain.

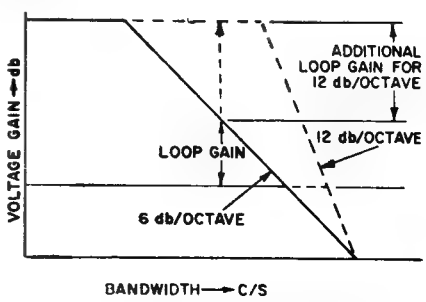


Fig 5 — Comparison of loop gain for 6 db/ and 12 db/ octave amplifiers.

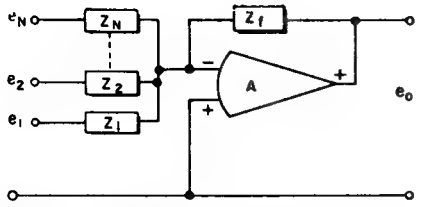
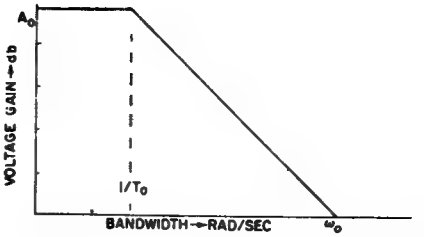


Fig 6 — Multiple input summing amplifier.



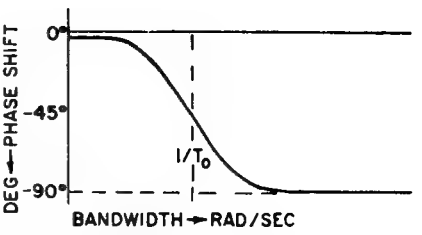


Fig 7 — Open loop gain phase response.

Frequency Response and Dynamic Errors

We have already mentioned that nature imposes some restrictions on the maximum achievable bandwidth for operational amplifiers. Typical amplifiers have unity gain bandwidth of 1 Mc/s with some special amplifiers having bandwidths as high as 100 Mc/s. Since operational amplifiers almost invariably employ large amounts of negative feedback, the attenuation of open loop response must satisfy certain requirements to insure stable closed loop operation. H. N. Bode in his "Network Analysis and Feedback Amplifier Design", D. Van Nostrand, Princeton, New Jersey 1951 showed that closed loop operation will be stable if the log plot of open loop gain exhibits a slope of less than—12 db/octave in the region of crossover.

Operational amplifiers are usually designed to have attenuation of 6 db/octave to assure that closed loop operation will be stable for all possible values of resistor feedback with the usual stray capacitance, load capacitance and input capacitance which are present in a circuit. However, there are advantages to be gained from amplifiers designed for 12 db/octave attenuation. The stability problem for these amplifiers can be solved, once a few basic application techniques are understood.

Fig 7 gives a very close approximation to the open loop gain-phase characteristics of a 6 db/octave amplifier. Mathematically, the amplifier behaves like a simple linear first order lag.

$$A(S) = A_o/(1 + T_oS), \text{ where } S = j\omega$$

For frequencies greater than $s = 1/T_o$, gain becomes,

$$A(S) = A_o/T_oS = \omega_o/S \qquad (14)$$

Substituting eq (14) for A in eq (5) the dynamic closed loop gain response for the circuit in Fig 1 becomes:

$$e_o/e_i = -\left[\frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + \frac{S}{\omega_o}\left(1 + \frac{Z_f}{Z_i}\right)}\right] \qquad (15)$$

$$= -\left[\frac{Z_f}{Z_i}\right]\left[\frac{1}{1 + T_cS}\right]$$

$$\text{where } T_c = [1 + Z_f/Z_i]/\omega_o = 1/\beta\omega_o \qquad (16)$$

Fig 8 illustrates the dynamic closed loop gain response given by eq (15). The closed loop bandwidth is directly proportional to open loop bandwidth ω_o and is inversely proportional to closed loop gain. This is another way of stating that the gain-bandwidth product for a feedback amplifier is constant. As closed loop gain is increased, bandwidth is decreased.

Transient Response: The closed loop step response for eq (15) is a simple exponential with time constant T_c:

$$e_o(t) = (-Z_f/Z_i)(1 - e^{-t/T_c})$$
$$\text{for } e_i = \mu_{-1}(t)$$

The time constant, T_c, eq (16), increases for increasing values of closed loop gain and decreases for increasing values of open loop bandwidth, ω_o. Fig 9 shows the step function response together with the time required to reach various percentages of the final values.

As an example, the time required for a one Mc/s unity gain (ω_o) amplifier connected for a closed loop gain of 100 to reach 0.1% of its final value after a step input,

$$T = 6.9T_c = 6.9(100/6.28 \times 10^6) = 110\ \mu\text{sec}$$

Rate Limiting, Slewing Rate and Full Output Frequency Response: Another limitation to transient response is rate limiting. Apart from bandwidth, operational amplifiers have limitations on the maximum rate of change of output voltage which will not permit the amplifier to respond as fast as the amplifier time constant might indicate. This tends to be a problem for large input voltage steps.

The maximum full output frequency is usually given by the manufacturers to define this limitation. Alternatively, a specification for maximum slewing rate is sometimes given, generally in volts/μsec. Slewing rate and full output frequency are related as follows: for a sine wave, the maximum output voltage for full output frequency, ω_{fo},

$e_o(t) = A_p \sin \omega_{fo} t$, *where* A_p *is the peak output voltage*

The maximum rate of change of this voltage or slewing rate is,

$$(de_o/dt)_{max} = A_p\omega_{fo}/10^6 \text{ volts/}\mu\text{sec}$$

Fast Roll-Off Amplifier: Not only do fast roll-off amplifiers provide more loop gain at high frequencies as previously discussed, but they also offer wider closed loop bandwidth for a given unity gain crossover frequency. Fig 10 shows a comparison of the closed loop bandwidths obtainable for a 6 db/octave and a 12 db/octave amplifier. Stable closed loop performance can be obtained for a 12 db/octave amplifier by the addition of a lead capacitor in the feedback network as shown in Fig 11. The effect of the lead capacitor on closed loop response is illustrated in Fig 12. So long as the rate of

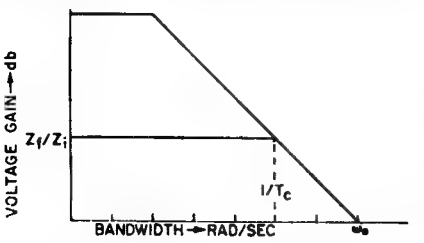


Fig 8 — Closed loop frequency response.

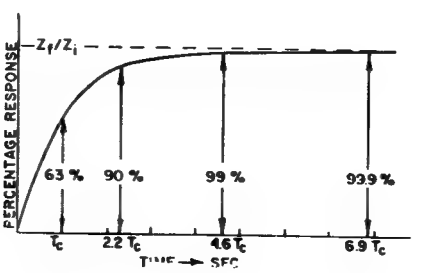


Fig 9 — Closed loop step response.

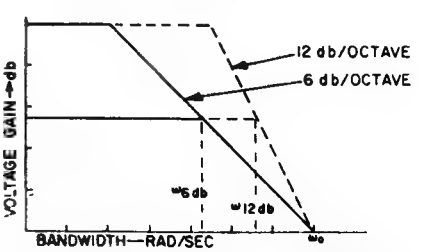


Fig 10 — Comparison of bandwidth for 6 and 12 db/ octave amplifiers.

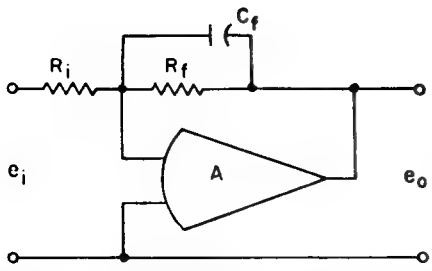


Fig 11 — Stabilization with feedback capacitor.

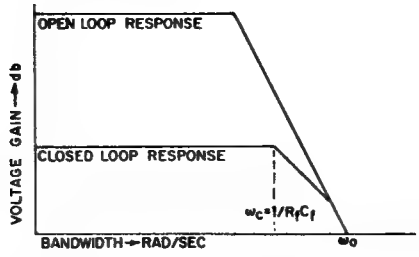


Fig 12 — Frequency response with feedback capacitor.

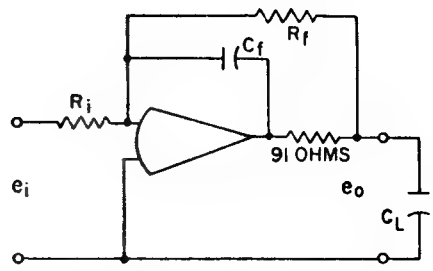


Fig 13 — Isolation of load capacitance.

closure between the open loop and closed loop response curves is less than 12 db/octave, the closed loop response will be stable. The location of the compensating break frequency, ω_c, establishes the closed loop phase margin.

Fig 13 illustrates a technique for isolating load capacitance which may cause oscillations for a 12 db/octave amplifier. Since the load isolation resistor is inside the feedback loop, low output impedance is maintained. These illustrations are intended to indicate that in most applications, a 12 db/octave amplifier can be stabilized as well as a 6 db/octave amplifier and at the same time, the benefits of increased loop gain at high frequencies and wider closed loop frequency response are obtained.

Overload Recovery: Another source of dynamic error is the overload recovery time after the amplifier has been saturated. Chopper stabilized amplifiers, by their very design, have notoriously long overload recovery times: up to 3 minutes. Differential amplifiers are in general much better in this respect with recovery times in the range from 5 to 50 msecs. Moreover, 12 db/octave amplifiers tend to recover faster than 6 db/octave amplifiers and may have recovery times as short as 200 μsec.

A remedy for the overload recovery problem is to include a circuit in the feedback loop which prevents the output from reaching the saturation voltage. One such clamping circuit is shown in Fig 14. This circuit has a response of a few μsec so that recovery time is generally limited only by the closed loop bandwidth of the amplifier. In addition, this configuration limits the leakage current through the feedback network to something less than 10 pa, depending on the quality of the diodes.

Input Offset and Drift Errors

Although an ideal amplifier has exactly zero output voltage for zero input voltage, any practical dc amplifier invariably exhibits an input offset. Offset in itself is generally not a serious problem since you may compensate for it with various techniques by artificially injecting an equal and opposite signal at the summing junction. However, any tendency for the offset to drift either due to temperature change, time or supply voltage variations, presents a basic limitation since this drift would necessitate the compensating signals to be constantly readjusted. One important figure of merit for an operational amplifier is the magnitude of offset drift.

Offset drift falls into two separate and distinct categories. One cause of drift can be characterized by a voltage source connected in series with the summing junction, Fig 15, while another source of drift can only be characterized by a current source in parallel with the summing junction. To successfully apply operational amplifiers the distinction between these two sources of drift must be understood in order to predict their effect on circuit performance.

Voltage Offset and Drift: The principal causes for voltage drift are changes in ambient temperature and supply voltage or long term stability due to component aging. Less obvious and more uncommon sources of voltage offset are self heating due to load variations and rectification of high frequency overdrive signals. Encapsulated amplifiers offering higher output voltage or current ratings are subject to considerable internal dissipation which may generate enough heat to cause the input to drift as the load is changed. Input signals which contain frequency components that exceed the amplifier bandwidth or rate limiting capabilities may be rectified and cause an offset referred to the input.

Voltage drift due to ambient temperature change is generally specified as the average drift over a given temperature range. This can be somewhat misleading. For example, Fig 16 shows a voltage offset vs temperature for a particular amplifier. Although the curve falls within the specification limits, the slope of the curve at any one temperature may exceed the average drift rate. A more precise way of specifying drift is to give the maximum total voltage change over the temperature range of interest.

Another anomaly in specifying temperature drift is that the ratings given are for steady state temperature conditions. The drift performance, particularly for differential type amplifiers, depends on precisely matching the temperature effects of the input transistors. Successful operation then depends on the components within the circuit being maintained at exactly the same temperature. Encapsulated amplifiers use potting compounds with low thermal resistance which tends to minimize thermal unbalance. However, in applications where thermal gradients are prevalent in the vicinity of the amplifier, it is possible to obtain voltage offset transients which exceed the steady state drift specifications by an order of magnitude. Chopper

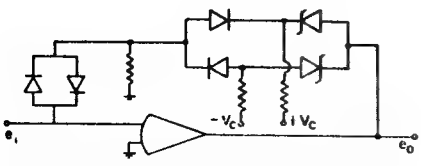


Fig 14 — Overload recovery circuit.

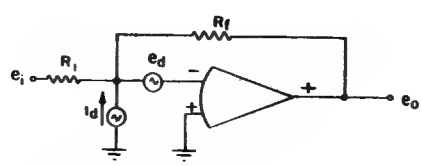


Fig 15 — Sources of offset drift.

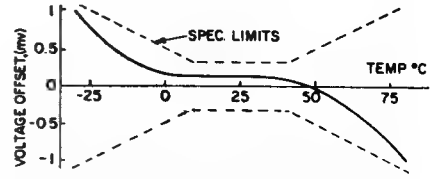


Fig 16 — Voltage drift vs temperature.

type amplifiers are relatively insensitive to thermal gradients and they should be considered in environments which present this problem.

Voltage source drift referred to the output for the circuit in Fig 15 is given by,

$$\Delta e_o = e_d/\beta = e_d(1 + R_f/R_i)$$

$$\Delta e_o \approx e_d R_f/R_i, \text{ for } R_f >> R_i \qquad (17)$$

where e_d is the total offset voltage change over the time, temperature and supply voltage range of interest. Eq (17) follows directly from eq (11) where it was indicated that the output is always $1/\beta$ times the error voltage at the summing junction. Since e_d can be considered another form of error voltage the same eq (11) is applicable.

Offset drift is defined in terms of the voltage required at the input to rezero the output. Thus drift referred to the input is obtained by dividing the output drift eq (17) by the closed loop gain, R_f/R_i,

$$\Delta e_i = (e_d/\beta)(R_i/R_f) = e_d(1 + R_f/R_i)(R_i/R_f)$$

$$\Delta e_i \approx e_d, \text{ for } R_f >> R_i \qquad (18)$$

It is important to note that the usual approximations for voltage source drift referred to the input and output as given by eq (17) and eq (18) can lead to substantial errors for low values of closed loop gains. To illustrate this point, the table, Fig 17 gives the exact values for input and output drift for various values of closed loop gain, R_f/R_i, for an amplifier with $e_d = 20$ μv/°C.

Closed Loop Gain R_f/R_i	Input Drift, μv/°C $e_i = e_d(1 + R_f/R_i)(R_i/R_f)$	Output Drift, μv/°C $e_o = e_d(1 + R_f/R_i)$
1	40	40
2	30	60
3	26	80
4	25	100
5	24	120
10	22	220
100	20.2	2020

Fig 17 — Voltage drift vs closed loop gain.

Current Offset and Drift: The discussion of voltage offset and drift in the previous section is applicable to current offset and drift as well, except for one important difference. Unlike voltage source drift, the effect of current drift depends on the magnitude of the feedback components since any current which is pumped into the summing junction is inherently balanced out by an equal and opposite current which forced through the feedback impedance, Z_f. Consequently, the uncertainty in output voltage due to a change in offset current i_d, is:

$$\Delta e_o = i_d R_f$$

By dividing the output voltage by closed loop gain, the uncertainty referred to the input is:

$$\Delta e_i = e_o/(R_f/R_i) = i_d R_i$$

Thus, to obtain the effect of current drift referred to the input, multiply the current drift by the summing impedance, R_i.

Current Drift Compensation: For differential type amplifiers it is possible in some applications to partially compensate for current drift. This follows as actually, each input of the amplifier has an effective parallel current drift source as shown in Fig 18. The current drift and offset at each input tend to track with changes in temperature, time and supply voltage. Therefore, if the impedance in each leg is balanced, the effect of current drift and offset tend to be cancelled.

The circuit in Fig 18, illustrates the connections for current drift compensation. For this circuit the current drift at the output is:

$$\Delta e_o = -i_{d2}(R_c)(R_i + R_f)/R_i + i_{d1}(R_f)$$

For the case where $R_c = R_f R_i/(R_i + R_f)$ this becomes:

$$\Delta e_o = R_f(i_{d1} - i_{d2})$$

Dividing the output drift by the closed loop gain $(-R_f/R_i)$, gives the drift referred to the inputs as:

$$\Delta e_i = R_i(i_{d2} - i_{d1})$$

Consequently, if the two current sources are exactly equal in magnitude and R_c is chosen correctly, current drift is entirely cancelled. Although this is never quite the case, at the extreme of operating temperatures where current drift is worst, you can obtain by this technique an improvement in current drift approaching a factor of ten.

Combined Voltage and Current Drift: Total drift, which is obtained by combining voltage and current drift, referred to input and output is:

$$\Delta e_i = e_d + i_d R_i \text{ and}$$

$$\Delta e_o = e_d \frac{R_f}{R_i} + i_d R_f, \text{ for } R_f >> R_i$$

It is informative to illustrate by an example, the relative importance of voltage and current drift. The chart, Fig 19 gives the total drift referred to the input of a typical differential amplifier with average voltage and current drift of 25 μv/°C and 0.5 na/°C respectively. Total drift is given for various values of summing resistor R_i.

Input drift for low impedance circuits is thus primarily due to voltage source drift, while for high impedance circuits, input drift is primarily due to current source drift. In conclusion, you must consider both the voltage and current source drift, together with impedance levels, in predicting the offset and drift performance of an operational amplifier.

Errors Due to Finite Input Impedance

The prior discussions have presumed that open loop input impedance is infinite. Actually, solid state operational amplifiers have input impedances which range from 100 KΩ to several MΩ. In most applications it is reasonable to neglect the effects of finite input impedance; however, in instances where the summing impedance, R_i, is comparable to or larger in value than the amplifier input impedance, the closed loop performance of the circuit is somewhat degraded. The primary effect of finite input impedance is to reduce loop gain.

The degradation in close loop performance due to finite input impedance is best explained in terms of feed-

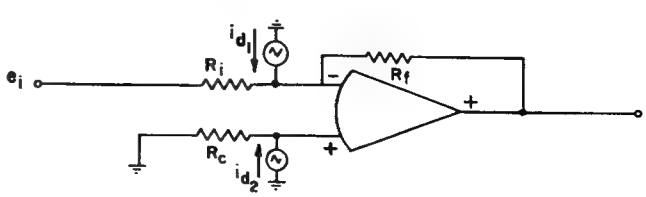


Fig 18 — Current drift compensation.

R_i KΩ	Δe_i due to e_d μV/°C	Δe_i due to i_d μV/°C	Total Δe_i μV/°C
1	25	0.5	25.5
10	25	5	30
100	25	50	75
1000	25	500	525

Fig 19 — Comparison of voltage and current source drift.

back attenuation (β). The circuit Fig 20 shows an amplifier with finite input impedance.

The calculation for β from eq (11) must be modified to account for the fact that Z_{IN} appears in parallel with Z_i in the feedback voltage divider.
If we let,

$$Z_x = Z_i \, Z_{IN}/(Z_i + Z_{IN}) \tag{19}$$

then from eq (11),

$$(\Delta e_o/\Delta e_i)(Z_x + Z_f)/Z_x = 1 + Z_f/Z_x = 1/\beta'$$

or

$$\beta' = \frac{1}{1 + (Z_f/Z_x)} \tag{20}$$

When Z_i becomes comparable to or higher in value than Z_{IN}, the value for feedback attenuation and consequently loop gain, Aβ′, is substantially reduced. For example, if a one megohm summing resistor were used with an amplifier with 100 KΩ input impedance, loop gain would be attenuated by approximately a factor of ten.

Fig 21 shows the effect of Z_{IN} on loop gain. A less obvious effect of finite input impedance is that the attenuation in loop gain also reduces closed loop bandwidth.

Finite Z_{IN}, does not affect closed loop gain, except by the increased errors due to reduced loop gain.

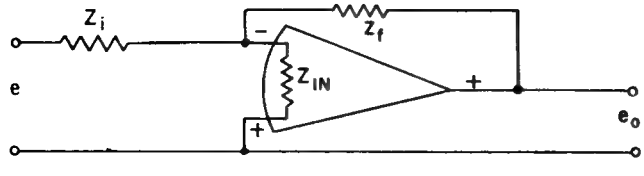


Fig 20 — Amplifier with finite input impedance.

Closed Loop Input Impedance

For the inverting connection, Fig 20, the closed loop input impedance is almost exactly equal to the summing impedance, Z_i, since the summing voltage is at virtually zero voltage. To be exact, the input impedance for this connection is,

$$Z_{icl} = Z_i + \frac{(Z_{IN}Z_f)/(Z_{IN} + Z_f)}{1 + AZ_{IN}/(Z_{IN} + Z_f)}$$

In the non-inverting connection, Fig 22, negative feedback is used to produce extremely high input impedance.

Closed loop input impedance for this configuration is:

$$Z_{icl} = Z_{IN}(1 + A\beta)$$

Theoretically, it is possible to obtain fantastically high input impedance in this way. However, common mode impedance and leakage resistance associated with the wiring and connectors tends to limit the attainable input impedance to generally 100 MΩ except for special very high input impedance amplifiers.

Errors Due to Non-zero Output Impedance

Open loop output impedance, Z_o, varies from as little as a few ohms to as much as several thousand ohms, with the majority of solid state amplifiers having 100 to 500 Ω output impedance. Output impedance forms a voltage divider with the load and feedback impedance which effectively attenuates open loop gain, A, which in turn reduces loop gain. The exact expressions for open loop gain taking output impedance into account is:

$$A' = \frac{A + (Z_o/Z_f)}{1 + \left[\frac{Z_f + Z_L}{Z_f Z_L}\right] Z_o} \approx \frac{A}{1 + \left[\frac{Z_f + Z_L}{Z_f Z_L}\right] Z_o} \tag{22}$$

Normally, manufacturers specify open loop gain at rated load with the assumption that $Z_f > Z_L$ so that in effect, a value for A′ is given. Open loop gain will vary slightly as the load impedance is changed. However, from eq (9) this variation is reduced by the loop gain in closed loop operation.

Output impedance will also cause additional phase shift with a capacitance load which tends to introduce stability problems. The circuit in Fig 13 shows a technique for correcting this difficulty.

Negative feedback reduces open loop output impedance by a factor approximately equal to the loop gain. Quantitatively, closed loop output impedance is:

$$Z_{ocl} = \frac{Z_o}{1 + A'\beta'}$$

Errors Due to Noise

Noise can be considered as any spurious output which is not contained in the input signal. Drift is merely a special case for noise which occurs at very low frequencies. The analysis of drift and the equations given to predict drift referred to the input and output are equally applicable to high frequency noise signals. In the general case, noise, like drift, can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction as depicted in Fig 15. Like drift, the effect of current

noise is directly proportional to the summing impedance.

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the frequency band for the specification is given.

Sources of Noise: Noise may appear at a discrete frequency, such as 60 c/s. It is usually picked up by electrostatic or electromagnetic coupling to the power lines or ac power transformers. In a chopper stabilized amplifier, there is usually noise generated at the chopping frequency. This noise may be produced by insufficiently shielded chopper drive leads or through electrostatic coupling within the chopper itself.

Noise can also arise from man-made RF interference. For example, the opening of a relay contact handling an inductive load may radiate sufficient energy to cause pulses of more than one volt peak to be generated across a three foot length of wire several feet away from the noise-generating circuit. The induced noise generally appears in the form of ringing at a frequency determined by the inductance and capacitance of the conductor that acts as a receiving antenna. While this ringing may appear in the region of 10 to 100 Mc/s, it may result in a low-frequency pulse output from a dc amplifier.

Because the base to emitter diode of a transistor amplifier stage is a rectifying junction, an RF noise input can be converted to a dc output. Thus transistor amplifiers are occasionally found to produce an audio output when in the vicinity of a strong broadcast station or may produce an audio pulse output due to an arcing relay.

RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. You can prevent noise pick-up by adequate shielding and the use of low-pass filters on all incoming leads connected with very short wires. Such filters generally have to be isolated from the feedback loop by adequate resistance in series with the input or output lead.

Random or statistical noise is generated in semiconductors and other components within an amplifier. "White" noise is a particular distribution of random noise which contains equal amounts of energy in each cycle of bandwidth. Such noise when generated by a resistor is termed "thermal" noise. The noise voltage generated by a transistor is generally white in the medium-high frequency region and increases in its energy per cycle at extreme high and low frequencies. Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to minimize random noise.

Thermal Noise: Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons, which generates minute voltages in a random

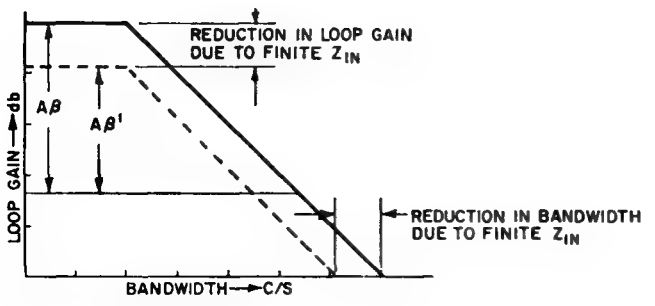


Fig 21 — Effect of Z_{IN} on loop gain and bandwidth.

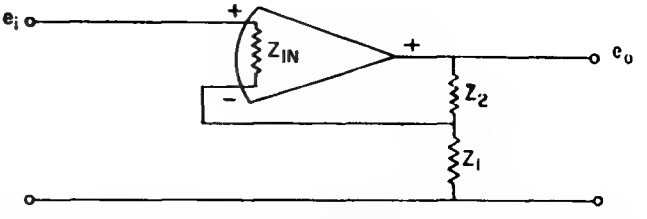


Fig 22 — Non-inverting connection for high input impedance.

manner across the terminals of the conductor or resistor. This noise voltage, sometimes referred to as "Johnson noise", is generated in the resistive component of any impedance and has a value:

$$E_n = \sqrt{4KT\,\Delta f R}$$

where E_n = the rms value of the noise voltage,
K = Boltzmann's Constant = 1.38×10^{-23} joules/°K,
T = absolute temperature of the resistance, °K,
Δf = the frequency band in which the noise is measured.

As a thumb rule, remember that a 1 kΩ resistor generates 1 μv rms in a 60 kc/s bandwidth. A 100 kΩ resistor generates 10 μv rms in the same bandwidth. The noise voltages generated by other values of resistance in other bandwidths can be calculated from these numbers by remembering that the noise is proportional to the square root of the resistance and the bandwidth.

Noise Specification: Although equivalent input noise voltage and noise current are most commonly used to characterize operational amplifier noise, there are several methods for specifying amplifier noise.

Equivalent Input Noise Voltage: It is convenient to separate the effects of equivalent input noise voltage and current. The equivalent input noise voltage of a dc amplifiers is that equivalent input noise voltage generated in series with a short circuit at the input terminals.

Equivalent Input Noise Current: When an amplifier is connected to a high impedance source, its noise output increases beyond that due to amplified noise voltage in the source resistance. When the source resistance becomes very large, the noise in a given bandwidth referred to the input becomes proportional to the source resistance. The increase in noise may be expressed in terms of an equivalent input noise current which causes a noise voltage drop across any large source resistance. Measurement of this noise current is generally made at such a high value of source resistance that the equivalent input noise voltage is much greater than that obtained with a shorted source.

Noise Figure: Noise figure is the ratio in db of the equivalent input noise power of the amplifier with a given source resistance over that noise power generated in the source resistance alone. For example, an amplifier having an equivalent input noise of 2 μv rms over a 60 kc/s bandwidth when connected to a 1 kΩ source resistor has a noise figure of 6 db because the equivalent input noise power is four times that of the source resistor alone.

Equivalent Input Noise Resistance: The equivalent input noise of an amplifier may be expressed in terms of the noise that would have been generated by a resistor connected in series with the input terminals of a noiseless amplifier. In the example above, the amplifier had an equivalent noise resistance of 3 kΩ which, when added to the source resistance of 1 kΩ, generated an equivalent input noise voltage of 2 μv rms. ■

OPERATIONAL AMPLIFIERS, PART II

Inverting, non-inverting and differential configurations

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Part I. Principles of Operation and Analysis of Errors appeared in the September issue of EMD.

Most operational amplifier circuits are constructed in one of three basic amplifier configurations—inverting, non-inverting or differential. The useful properties of all three configurations depend on the virtues of negative feedback coupled with extremely high open loop voltage gain. The configurations differ only in the manner in which the input signal is applied and the feedback components are arranged. The relative merits and limitations of these three basic configurations are discussed in this article.

INVERTING CONFIGURATION

The characteristics of the inverting configuration (Fig 23) were analyzed in Part I and will not be repeated here but a summary of the essential advantages and disadvantages is presented.

Highest accuracy can generally be obtained with the inverting amplifier, since, unlike the non-inverting amplifier, one input is normally grounded and there are no common mode voltage errors. Single ended amplifiers, which require that one input be grounded, can be used only in the inverting connection. This includes most chopper stabilized type operational amplifiers. For ac amplifiers you can obtain the lowest distortion in the inverting mode since common mode voltage errors also introduce distortion. The inverting configuration is excellent for summing two or more input signals. This follows as the summing junction is virtually at ground potential so that the input signals are almost completely isolated from each other.

Another versatile feature of the inverting amplifier is that it is possible to obtain closed loop gains less than one; which is not possible with the non-inverting amplifier. In many applications such as active filters, servo amplifiers and integrators you must attentuate a portion of the frequency response below unity gain.

Closed loop input impedance, for the inverting amplifier, which is essentially equal to the summing impedance, Z_1, is limited to a few megohms for all practical purposes. This follows, because as a rule of thumb, the summing impedance should not be much greater than the amplifier's open loop input impedance, Z_{IN}, which for most solid state operational amplifiers is in the range from 0.1 to 1 megohm. Another limitation is that the inverting configuration for very low closed loop gains degrades voltage source drift and noise by as much as a factor of two for unity gain. This degradation in drift and noise does not occur for the non-inverting configuration. The inverting configuration is a poor choice if you require both high input impedance and wide bandwidth. When using large summing and feedback resistors, stray capacitance has a greater effect in limiting closed loop bandwidth.

Low Input Impedance

Negative feedback reduces the input impedance at the summing junction of the inverting amplifier to negligible proportions. You can use this characteristic to advantage in some applications such as amplifying the output from photocells and other current generator type transducers. In analyzing circuits of this type it is convenient to treat the input signal as a current source as shown in Fig 24. Closed loop gain from a current source with infinite source impedance, is:

$$e_o/i_s = -(Z_f)\frac{1}{1+1/A\beta} \approx -Z_f \text{ for } A\beta >> 1$$

$$\text{where } 1/\beta = 1 + \frac{Z_f}{Z_{IN}} \text{ and } A \text{ is the open loop gain.} \quad (23)$$

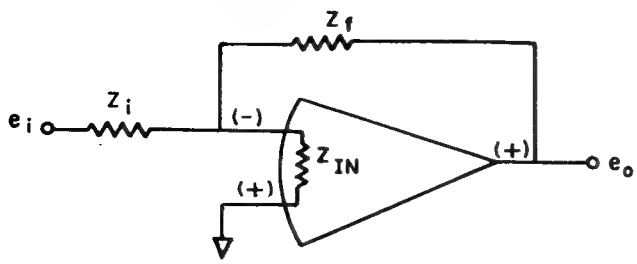

Fig 23 — Inverting configuration.

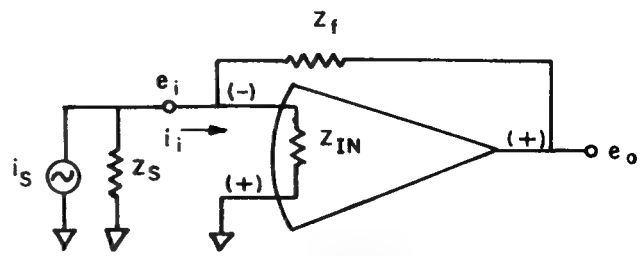

Fig 24 — Current source amplifier.

We see that if loop gain, Aβ, is sufficiently large, the value of the feedback resistor, Z_f entirely determines the gain. Closed loop input impedance is:

$$Z_i = \frac{e_i}{i_i} = \frac{\left(\frac{Z_f \cdot Z_{IN}}{Z_f + Z_{IN}}\right)}{(1 + A\beta)} \qquad (24)$$

When the source impedance, Z_s, becomes equal to or less in value than the open loop input impedance Z_{IN}, in parallel with the feedback impedance Z_f, you attenuate loop gain For finite, Z_s, modify eqs (23) and (24) by substituting $1/\beta'$ for $1/\beta$ where:

$$1/\beta' = 1 + \frac{Z_f(Z_s + Z_{IN})}{Z_s Z_{IN}} \qquad (25)$$

The effect of voltage and current drift for the circuit in Fig 24 is more revealing when referred to the output. Drift at the output is:

$$\Delta e_o = e_d\left(\frac{Z_s + Z_f}{Z_s}\right) + i_d Z_f \qquad (27)$$

where e_d is the voltage source drift, i_d is the current source drift.

NON-INVERTING CONFIGURATION

The most useful property of the non-inverting amplifier is the extremely large input impedance developed by negative feedback. Consequently, this configuration is most usful as a buffer or impedance transformation amplifier and for amplifying signals from very large source impedances.

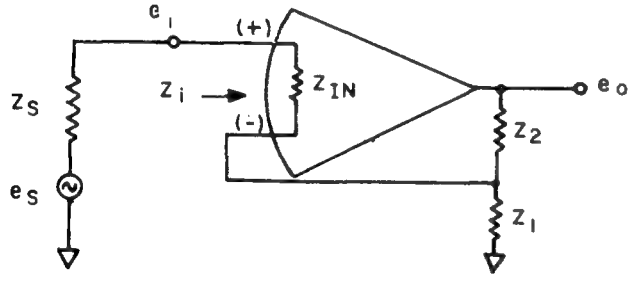

Fig 25 — Non-inverting configuration.

In this configuration, the input signal feeds to the non-inverting input and feedback returns to the inverting input as shown in Fig 25. Since negative feedback maintains the error voltage between the amplifier inputs to an infinitesimal value, you see that the negative input must follow any changes applied to the positive input. Therefore, the successful performance of this circuit requires a differential input amplifier where both inputs can operate above ground potential and where the rejection of common mode voltage is very good. Since most chopper stabilized operational amplifiers are single ended, you can not use them in this circuit.

Closed Loop Input Impedance

The high input impedance of the non-inverting connection is due to what is basically potentiometric feedback where the output signal or some fraction thereof is summed in series with the input. Consequently, the only input current which flows is due to the error voltage

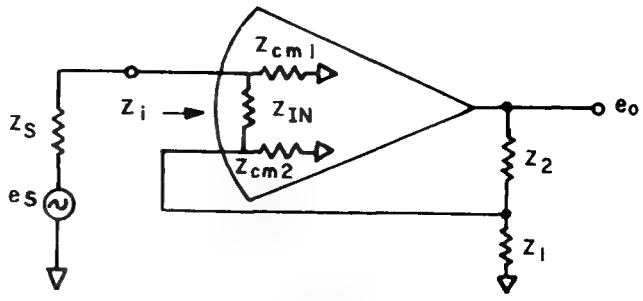

Fig 26 — Non-inverting amplifier with common mode input impedance.

across the amplifier's open loop input impedance Z_{IN}. Quantitatively, eq (28) gives the closed loop impedance if you assume that Z_{IN} is greater than the parallel impedance of Z_1 and Z_2.

Then,

$$Z_i = Z_{IN}\left[1 + A\beta\right] = Z_{IN}\left[1 + A\left(\frac{Z_1}{Z_1 + Z_s}\right)\right] \qquad (28)$$

Notice from eq (28) that Z_1 depends only on the ratio of $Z_1/(Z_1 + Z_2)$. Therefore, the magnitudes of Z_2 and Z_1 can be quite low without affecting input impedance, their magnitude being limited only by the output current rating of the amplifier. This situation offers two distinct advantages as compared to the inverting amplifier. First, for circuits requiring high gain and high input impedance, you can select resistors in a range of values where high quality, stable components are readily available. Secondly, you can design high input impedance, wideband amplifiers since stray capacitance has a smaller effect with the relatively low impedances which can be used for the feedback components.

From eq (28) you would expect input impedance to approach infinity as open loop gain, A, becomes very large. This would be true if it were not for common mode input impedance. In addition, to the impedance between amplifier inputs, Z_{IN}, there is also an effective impedance from each input to ground as shown in Fig 26. The parallel sum of the impedances from each input to ground, generally specified as the common mode input impedance, is Z_{cm} where:

$$Z_{cm} = \frac{Z_{cm1} \cdot Z_{cm2}}{Z_{cm1} + Z_{cm2}}$$

For transistor type differential amplifiers, common mode impedance generally ranges from 10 to 500 megohms and it is this value which sets the upper limit on the closed loop input impedance, Z_i, which can be achieved in the non-inverting configuration. Note that the output supplies the current for Z_{cm2} so that only Z_{cm1} draws input current. Therefore, the expected limit on closed loop impedance would be twice the specified common mode impedance, Z_{cm}.

At high frequencies three factors pose additional limits on the achievable input impedance.

- Lower open loop gain at higher frequencies reduces the negative feedback which causes the high input impedance.

- Shunt capacitance across the inputs reduces open loop input impedance at high frequencies.

- Shunt capacitance to ground reduces common mode impedance at high frequencies.

Closed Loop Gain

Assuming infinite input impedance, closed loop gain is:

$$\frac{e_o}{e_s} = \underbrace{\left[\frac{Z_1 + Z_2}{Z_1}\right]}_{\substack{ideal \\ amplifier}} \underbrace{\left[\frac{1}{1 + 1/A\beta}\right]}_{\substack{error\ due\ to \\ finite\ gain}}$$

$$\approx \left(\frac{Z_1 + Z_2}{Z_1}\right)\left(1 - 1/A\beta\right) \qquad (29)$$

where $1/\beta = (Z_1 + Z_2)/Z_1$ is the ideal closed loop gain, A is the open loop gain and the factor $A\beta$ is the loop gain. As for the inverting configuration, gain error is inversely proportional to loop gain. Eq (29) shows that with infinite $A\beta$, you cannot attenuate the closed loop gain below unity for any frequency. Unity gain occurs when $Z_1 = \infty$ and $Z_2 = 0$.

Gain for finite open loop input impedance, Z_{IN}, is,

$$\frac{e_o}{e_s} = \left[\frac{Z_1 + Z_2}{Z_1}\right]\left[\frac{1}{1 + 1/A\beta'}\right]$$

$$where\ 1/\beta' = \left(\frac{Z_1 + Z_2}{Z_1}\right)\left(\frac{Z_{IN} + Z_s}{Z_{IN}}\right) \qquad (30)$$

Consideration of common mode input introduces a further error in the closed loop equation. To a first approximation you should look at the effect of common mode impedance as forming a voltage divider to ground with source impedance, Z_s. This case modifies the gain equation to:

$$\frac{e_o}{e_s} = \left(\frac{Z_1 + Z_2}{Z_1}\right)\left(\frac{2Z_{cm}}{2Z_{cm} + Z_s}\right)\left(\frac{1}{1 + 1/A\beta'}\right) \qquad (31)$$

Common Mode Voltage Errors

Common mode voltage rejection is a source of error for the non-inverting configuration which is not a problem for the inverting connection. Ideally, for a differential input amplifier, the gain from each input to the output is exactly equal and opposite so that no output is produced when the same voltage is applied to both inputs. When the gains of each input are not exactly balanced, an output will be produced for a common mode input voltage. This output error, generally referred to the input as a ratio of the applied common mode voltage, is the common mode rejection ratio (CMR).

Since both inputs of a non-inverting amplifier assume approximately the same voltage, you would expect an input error equal to the CMR times the input voltage. The limit of the maximum input voltage is generally specified as the maximum common mode voltage.

Voltage Drift and Offset

Unlike the inverting amplifier, input voltage source drift (and noise) referred to the source voltage is independent of closed loop gain for the non-inverting amplifier. Thus for unity gain, voltage drift is improved by a factor of two as compared to the inverting amplifier.

Current Drift and Offset

The effect of current source offset and drift depends primarily on the magnitude of the source impedance. As shown in Fig. 27 offset current required by the plus input must be drawn through the source resistance. This produces an input offset voltage proportional to the product of offset current, i_d, and the source resistance, Z_s.

$$\Delta e_s = i_d Z_s$$

For very large source impedance, the magnitude of initial offset current and current drift is a very important consideration in selecting an amplifier. For example, an amplifier with any initial offset current of 10 na and current drift of 1 na/°C when used with a source impedance of

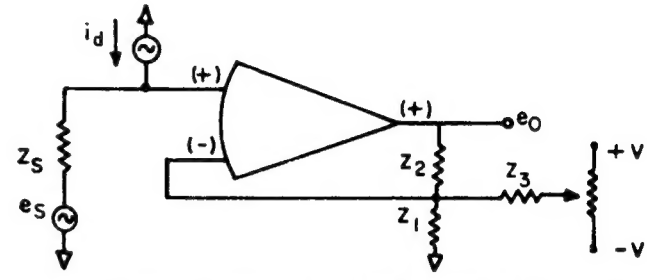

Fig 27 — Balance circuit for offset current ($Z_3 >> Z_1$).

10 megohms will produce an input offset voltage of 100 mv and drift of 10 mv/°C.

To bias out the initial offset current, sum an equal and opposite current to the non-inverting input as shown in Fig 28. However, the biasing network used in this scheme tends to lower the input impedance. Fig 27 shows a preferred circuit for zeroing large voltage offset due to input current which does not affect input impedance.

It is important to realize that the external zero voltage adjustment provided with many amplifiers is intended for balancing the amplifier's initial offset voltage and it should not be used to compensate for large voltage offsets due to offset current. The reason is that you may increase drift by intentionally generating a large voltage offset within the amplifier to compensate for current offset.

To reduce the effect of initial current offset and drift in some cases, add a resistance equal to the source impedance in series with the inverting input. Since offset current at each input is generally about equal and tends to track with temperature change, equalizing the impedance in both input leads cancels the effects of current drift to the extent that the input currents track. The limitation here is that as Z_s becomes greater than the open loop input impedance Z_{IN}, loop gain is lost. Moreover, large impedance in the inverting input tends to restrict the bandwidth due to stray capacitance and to generate excessive noise.

For the inverting amplifier, drift errors due to current offset, i , increase proportional to closed loop input impedance, since the summing impedance, Z , determines both the input impedance and the drift errors (i Z). However, for the non-inverting amplifier drift errors due to current offset is only a function of the source impedance (i Z) and is independent of closed loop input impedance. Usually the non-inverting amplifier is considered as a means of obtaining higher input impedance, but from this analysis we can see that another and equally important consideration by selecting the non-inverting configuration is to obtain lower overall drift errors for a given source impedance.

Non-Inverting ac Amplifier

When a blocking capacitor is used to ac couple the input to the non-inverting amplifier, a dc path must be provided for the input current as shown in Fig 28. Returning the leakage resistor to ground or preferably to a bias voltage, generates an equal and opposite current to null the initial offset current. The closed loop gain amplifies any offset voltage developed by input current to produce an output offset which tends to limit the output dynamic range. The maximum value for use for leakage resistance, R_L, is limited by the magnitude of current drift, the closed loop gain and the required output dynamic range.

Limitations on Maximum Source Impedance

Several factors have been mentioned which limit the maximum source impedance which can be used with a given set of amplifier specifications. The major considerations are:

- Loop gain is attenuated when the source impedance exceeds the amplifier's open loop input impedance, Z_{IN}. The magnitude of this attenuation is $Z_{IN}(Z_{IN} + Z_s)$. Gain accuracy, gain stability and closed loop input impedance are all degraded by loss of loop gain.
- The effect of input current noise is proportional to the magnitude of source impedance and excessive input noise can be generated for very large Z_s.

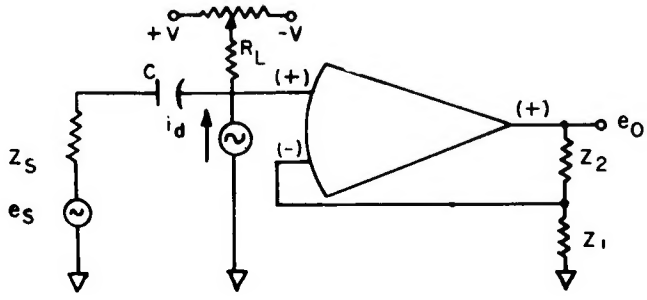

Fig 28 — AC non-inverting, with current offset adjust.

- Input voltage drift is produced which is proportional to the product of source impedance and current source drift.
- When the source impedance, Z_s, becomes comparable to or greater than the common mode impedance, Z_{cm}, an additional error is introduced into the closed loop gain; the error factor being:

$$\frac{2\ Z_{cm}}{2\ Z_{cm} + Z_s}$$

In conclusion, open loop input impedance, both common mode and differential, current source drift, noise and offset and open loop gain are the principle amplifier specifications which limit the maximum source impedance which can be used with the non-inverting configuration.

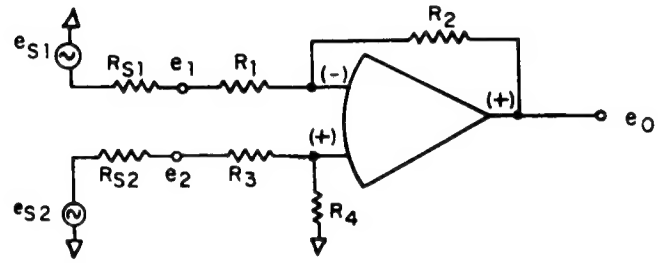

Fig 29 — Differential configuration.

DIFFERENTIAL CONFIGURATION

Ideally, the differential configuration shown in Fig 29 amplifies only the potential difference between e_1 and e_2. Voltages of the same potential, so-called common mode voltage, are not amplified. This configuration is useful in such applications as amplifying signals which are floated above ground potential, substracting voltages and measuring resistance bridge signals. The circuit can also amplify small signals in the presence of common mode noise voltage. Closed loop gain, for an infinite gain amplifier is:

$$e_o = e_2\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) - e_1\left(\frac{R_2}{R_1}\right) \qquad (33)$$

Except in applications, such as substracting, which require a scale factor difference, adjust the ratios R_2/R_1 and R_4/R_3 to be equal. In this case eq (33) becomes:

$$e_o = \left(\frac{R_2}{R_1}\right)(e_2 - e_1) \text{ for } \frac{R_1}{R_2} = \frac{R_3}{R_4} \qquad (34)$$

Closed loop input impedance for e_1 is just the summing resistor, R_1, while for e_2 it is $(R_3 + R_4)$. Like the inverting amplifier, the differential amplifier sometimes suffers from the relatively low input impedances which can be achieved. Fig 30 shows one arrangement of amplifiers which combines the high input impedance of the non-inverting amplifier with the common mode rejection capabilities of the differential amplifier. Gain for this circuit is:

$$e_o = \left(1 + x + y\right)\frac{R_2}{R_1}(e_2 - e_1) \qquad (35)$$

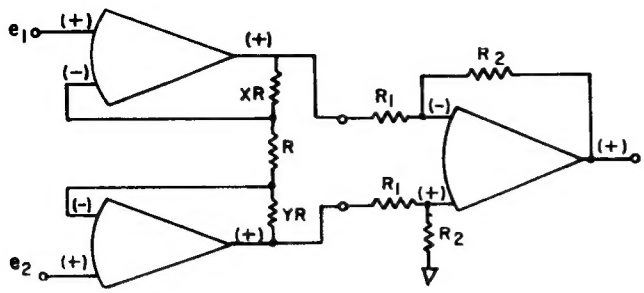

Fig 30 — Circuit for differential, high input impedance.

Common Mode Voltage and Rejection Ratio

The circuit of Fig 29 requires a differential input type amplifier where both inputs are operable above ground potential and where the rejection of common mode voltage at the two inputs is very good. Both inputs are constrained by negative feedback to be at essentially the same potential which is (e_2) ($R_4/R_3 + R_4$). If we call E_{cm} the maximum common mode voltage which the amplifier input terminals can withstand, then the maximum common mode voltage which can be applied to e_1 end e_2 is,

$$e_{1,2}\ max. = E_{cm}\frac{R_3 + R_4}{R_4} \qquad (36)$$

Common mode rejection ratio (CMR) is defined as the applied common mode voltage divided by the resulting error referred to the input. CMR for the circuit in Fig 29 depends on several factors which are discussed separately below. We shall assume here that $R_1 = R_3$ and $R_2 = R_4$.

Source Impedance Unbalance: An unbalance in source impedance will cause a common mode voltage error. The CMR, due to a small unbalance in source impedance is:

$$CMR = \frac{R_{s2} + R_3 + R_2}{(R_{s1} + R_1) - (R_{s2} + R_3)} \qquad (37)$$

$$For\ R_1 = R_3,\ R_2 = R_4,\ R_{s1} = R_s,\ R_{s2} = R_s - \Delta R_s$$

$$and\ R_s >> \Delta R_s$$

$$CMR \approx \frac{R_s}{\Delta R_s}\left(1 + \frac{R_1 + R_2}{R_2}\right)$$

Hence a given percentage unbalance in R_s will have a smaller effect on CMR when $(R_1 + R_2) >> R_s$.

Summing Impedance Mismatch: A common mode error is also introduced by a mismatch in the summing impedances, R_1 and R_3. Use eq (37) to predict the CMR due to this mismatch. Assuming $R_{s1} = R_{s2} = R_s$, $R_3 = R_1 - \Delta R_1$, and $R_1 >> \Delta R_1$, then eq (37) becomes:

$$CMR \approx \frac{R_1}{\Delta R_1}\left(1 + \frac{R_s + R_2}{R_1}\right)$$

Feedback Impedance Mismatch: A mismatch in R_2 and R_4 will cause a common mode voltage error for which CMR is given by eq (38).

$$CMR = \left(\frac{R_1 + R_4 + R_{s1}}{R_4 - R_2}\right)\left(\frac{R_2}{R_1 + R_{s1}}\right) \qquad (38)$$

Assuming

$$R_{s1} = R_{s2} = R_s,\ R_4 = R_2 + \Delta R_2\ and\ R_2 >> \Delta R_2$$

then eq (38) becomes,

$$CMR = \frac{R_2}{\Delta R_2}\left(1 + \frac{R_1 + R_s}{R_2}\right)\left(\frac{R_2}{R_1 + R_s}\right) \qquad (39)$$

From eq (39) we see that a circuit with higher gain, R_2/R_1, will have a higher CMR for a given percentage unbalance, $R_2/\Delta R_2$.

Amplifier Common Mode Rejection: The inherent common mode rejection of the amplifier itself will limit the common mode rejection of the circuit to that of the amplifier. Note that unbalancing the resistors R_1 and R_3, or R_2 and R_4, cancels the common mode error and effectively increases the CMR to infinity. The residual signal due to a common mode voltage will then consist of only distortion components arising in the input stage of the amplifier as it swings over the common mode voltage range.

AC Common Mode Rejection: When used to reject ac common mode voltages, unbalance of stray capacitance between each input and ground can cause a common mode voltage error. CMR due to stray capacitance is given by:

$$CMR = \frac{(R_p + jX_1)(R_p + jX_2)}{R_p(jX_1 - jX_2)} \qquad (40)$$

where $R_p = R_1R_2/(R_1 + R_2)$, jX_1 is the reactance to ground from input e_1 due to stray capacitance and jX_2 is the reactance to ground from input e_2.

Voltage and Current Drift

Offset and drift for the differential configuration are very much the same as for the inverting configuration which was discussed in Part I Sept EMD. In most differential amplifiers, the parallel sum of the impedances from each input to ground is balanced. Since the current at each input tends to track the other with changes in temperature, voltage offset due to current drift is cancelled to the extent that the currents do track.

OPEN LOOP OPERATION AND VOLTAGE COMPARATORS

In some applications you use the extremely high sensitivity of operational amplifiers, due to high open loop gain, with little or no feedback. In this case, the operational amplifier operates basically as a switch, since output is saturated at either the maximum positive or negative output voltage and a very small input voltage will cause the output to change polarity. Voltage comparators, used in digital voltmeters, analog-to-digital converters and precise timing circuits, are the most common application of operational amplifiers in the open loop mode. Fig 31 shows a simplified circuit for a voltage comparator.

The input signal, e_1, and the reference signal, e_{ref}, must be of opposite polarities. As the input voltage exceeds the reference voltage, a very small difference will cause the output to rapidly switch polarity. The threshold, or volt-

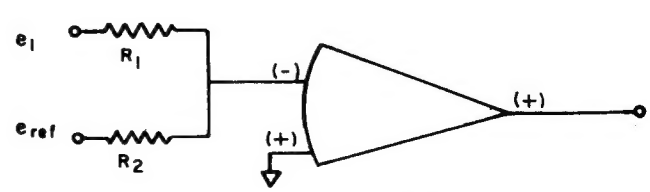

Fig 31 — Voltage comparator circuit.

age difference required to switch the output, depends on the maximum swing of the output voltage and the open loop gain of the amplifier. For example, if the maximum output swing were ±10 v and the open loop gain were 100,000, a 100 μv difference between the input and reference voltage would switch the output polarity. For a 100 v reference signal, this gives the circuit the ability to compare voltages to within one part in 10^6.

If you slowly vary the input voltage, any noise appearing on the input signal, the reference voltage or any noise picked up by the summing junction or generated within the amplifier itself will cause the output to chatter at the time of coincidence. Fig 32 shows how to eliminate this chattering by the use of positive feedback, which provides a hysteresis exceeding the noise level.

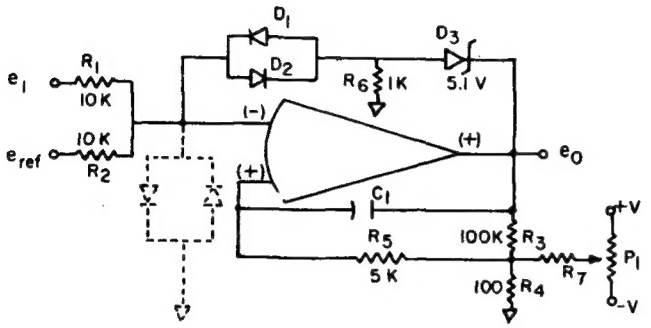

Fig 32 — Voltage comparator with hysteresis ($R_7 >> R_4$).

The zener diode feedback limits the amplifier output swing to —0.5 to 5 v. As the input voltage approaches the trigger level, the regenerative feedback due to switching the output causes a step in the net voltage of the positive input equal to one-thousandth of the output voltage change, or 5.5 mv. If the input noise level is less than 5.5 mv peak-to-peak, there will be no chattering of the output as a result of noise for a monotonic change of e_1 due to the bias generated at the positive input. Adjust the amount of hysteresis by changing the zener diode voltage or the ratio of R_3 and R_4. Add the resistor, R_5, in the positive input to balance the impedances of both amplifier inputs to ground, thereby reducing input offset due to current drift. Use the bias circuit formed by R_7 and P_1 to zero initial input offset.

Diodes D_1 and D_2 reduce leakage current to the summing junction which is generated by the zener diode, D_3. To some extent, depending on the values of R_2, R_6 and e_{ref}, these diodes also protect the summing junction from overloads. However, for very large reference voltage and small R_2 it may be desirable to add a pair of low leakage silicon diodes from the summing junction to ground to prevent damage or saturation of the amplifier input for large unbalance between the input signal and the reference voltage. With protecting diodes to ground and stable summing resistors, excellent performance is possible with hundreds of volts unbalance. The clamping feedback circuit also prevents the amplifier from saturating which guarantees rapid recovery in switching the output. The capacitor, C_f, speeds the switch action of the regenerative feedback and improves closed loop stability for some amplifier types.

Errors In Comparator Circuits

We have already mentioned that one error in the comparator's operation is the amount of error voltage required at the summing junction to switch the output. Most operational amplifiers have sufficient open loop gain so that this error is small compared to that due to noise and drift. Noise for obvious reasons limits the threshold of comparison and hysteresis should be used which is greater than the peak-to-peak noise at the summing junction from all sources including the signal and reference voltages.

Input offset drift, of course, shifts the level of coincidence between the input signal and the reference signal and thereby introduces an error in the absolute voltage as well as the repeatability of comparison. The factors contributing to input offset drift are the same as though the amplifier were used as a linear inverting amplifier and can be predicted from the amplifier's specifications and other considerations previously discussed. The same techniques that minimize drift in linear dc amplifier circuits should be used in comparator circuits. Namely, the summing impedance should be as low as possible, the impedances of each input of a differential amplifier should be balanced and summing impedances greater than the open loop input impedance of the amplifier should be avoided. With differential type amplifiers, noise and drift errors below 1 mv can be readily obtained and with chopper stabilized amplifiers, errors less than 50 μv are possible. Frequently these low errors are exceeded by noise and drift in the input and reference signals.

Response Time

When the input signal is changing rapidly through the trigger point, there may be a delay in the output switching due to the frequency response characteristics of the amplifier. While you can sometimes compensate the delay by a change in the reference voltage, this delay is frequently a function of temperature. For this reason, you obtain best high speed operation with amplifiers having wide gain bandwidth. Actually slewing rate or, alternatively, full output voltage response is the most significant specification, since rate limiting generally restricts the response time.

Overload recovery time can also introduce a delay in response. Therefore, the amplifier used must either have very fast recovery time or a circuit like that in Fig 32 must be used which prevents output overload and therefore any delay due to overload recovery. ■